

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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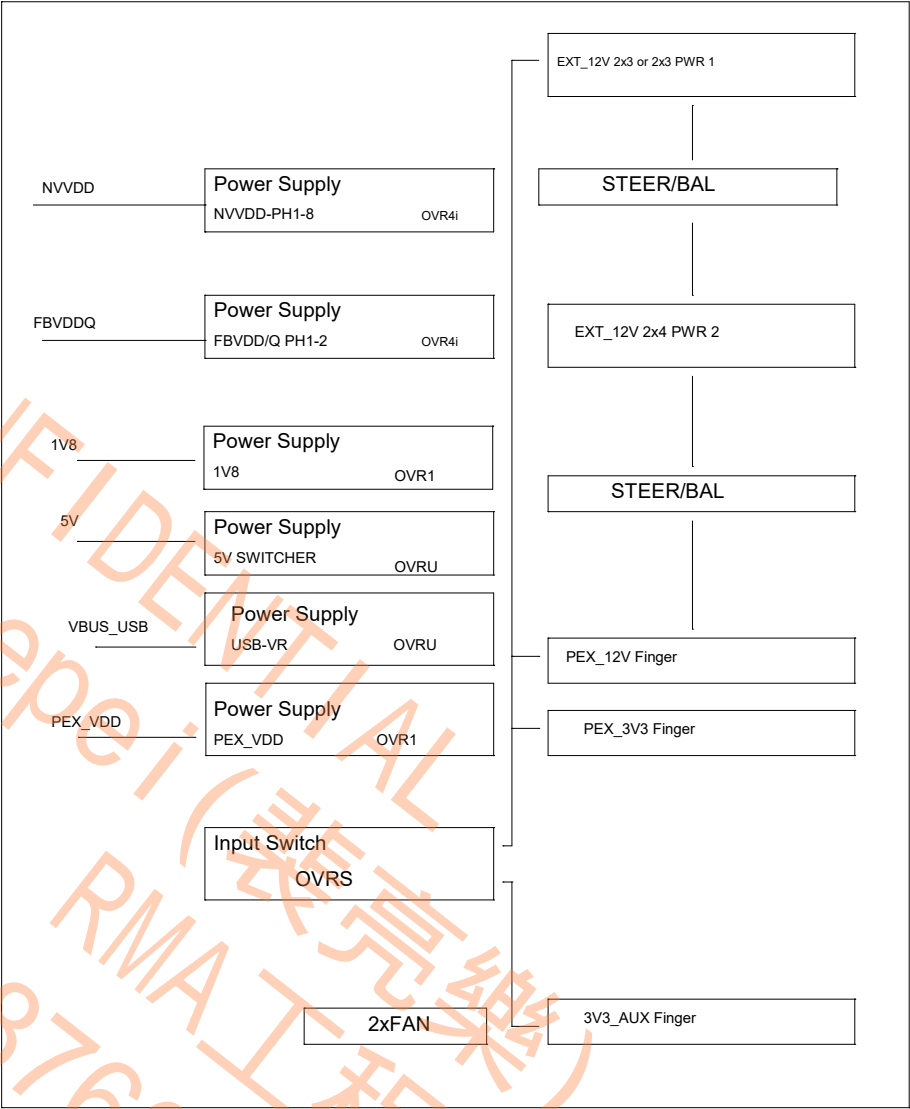
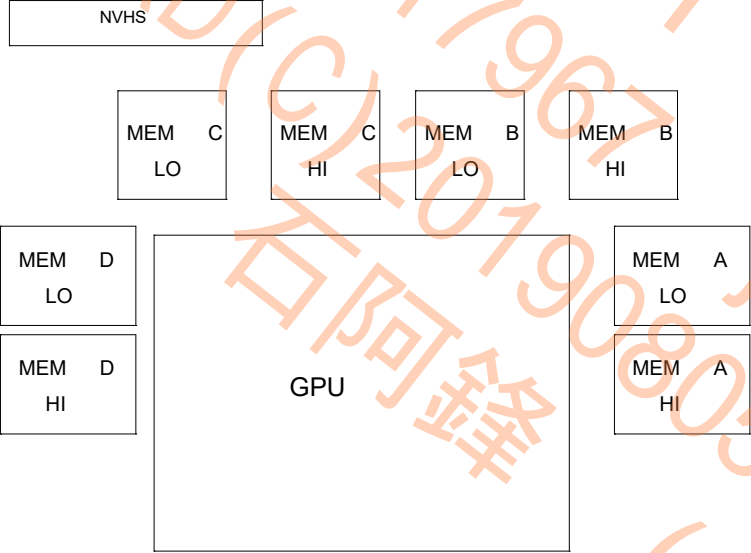
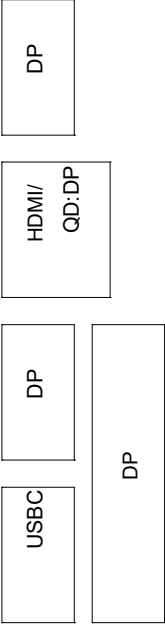
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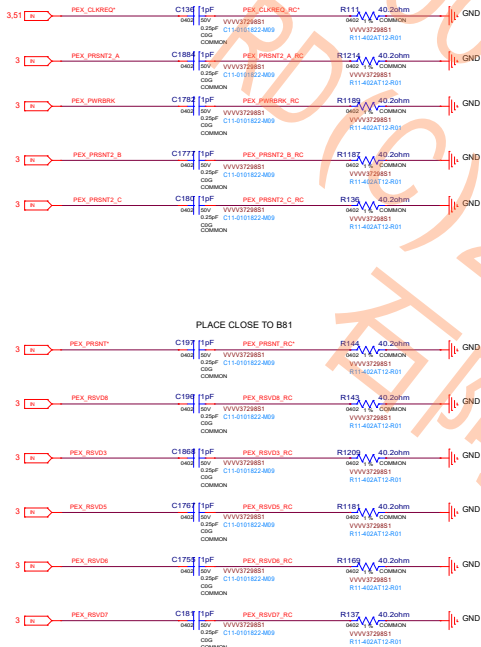
V372-3.0 change List
18 Change J4 footprint
19 Change J3 footprint
20 Remove DP co-layout
21 Remove JTAG & unused GPIO
32 Remove 0031_PS_FBVDD CONTROLLER OVR3
34 NVVDD CONTROLLER change to MP2888A
35 DRMos change to 10phases
36 DRMos change to 10phases
37 Add NVVDD Output CAP
41 Remove INPUT SWITCH Rail Balance
44 J8 change to 8pin
Add Fuse F1~F3
Change 12V input choke footprint
45 Add Hot Unplug Detect for J8
52 Add Remove LED & Fan Vin_12V option
53 Add MCU IT8295 for RGB LED

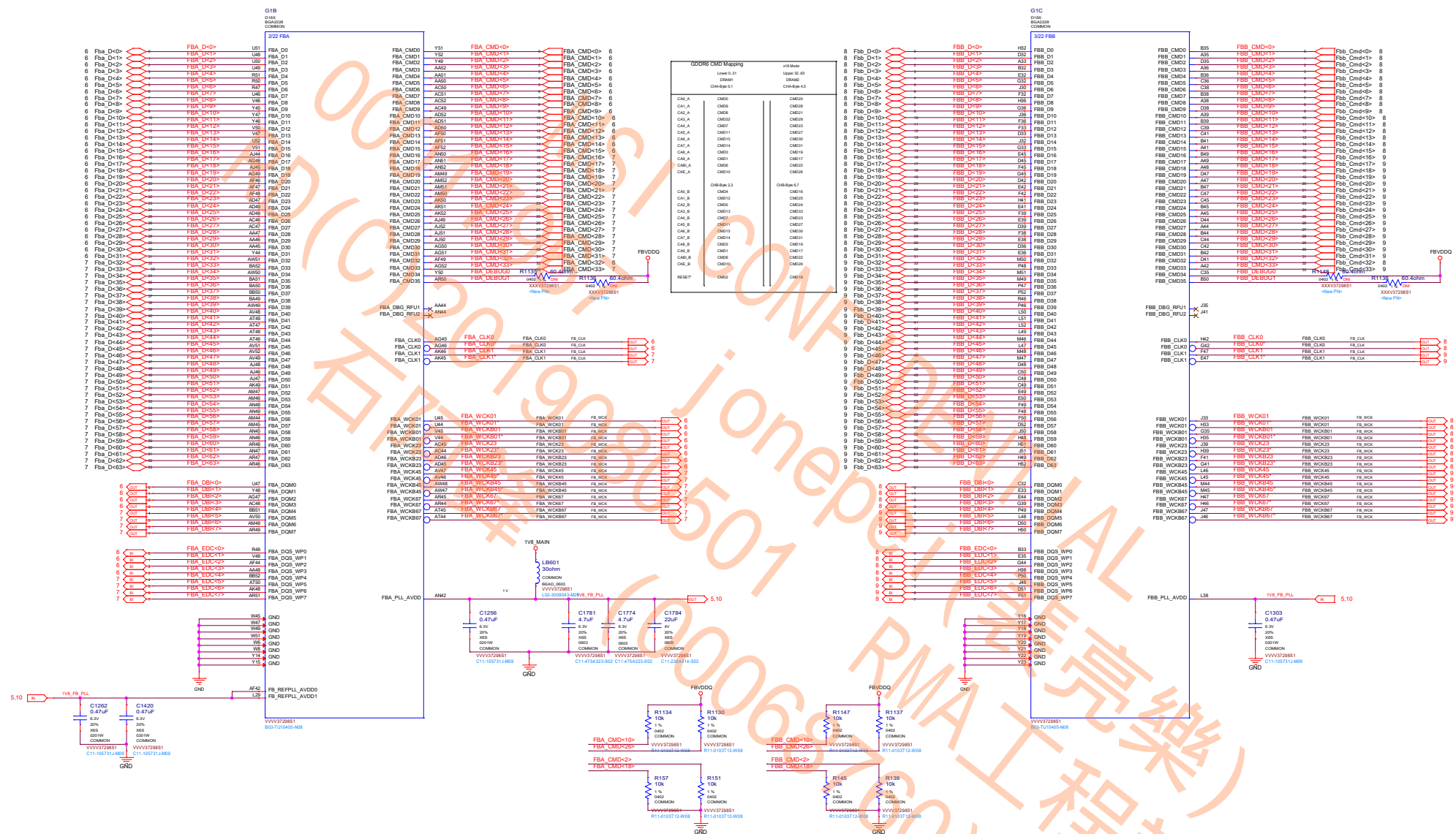
V372-3.1 change List
Base on V372-3.0 · No changed

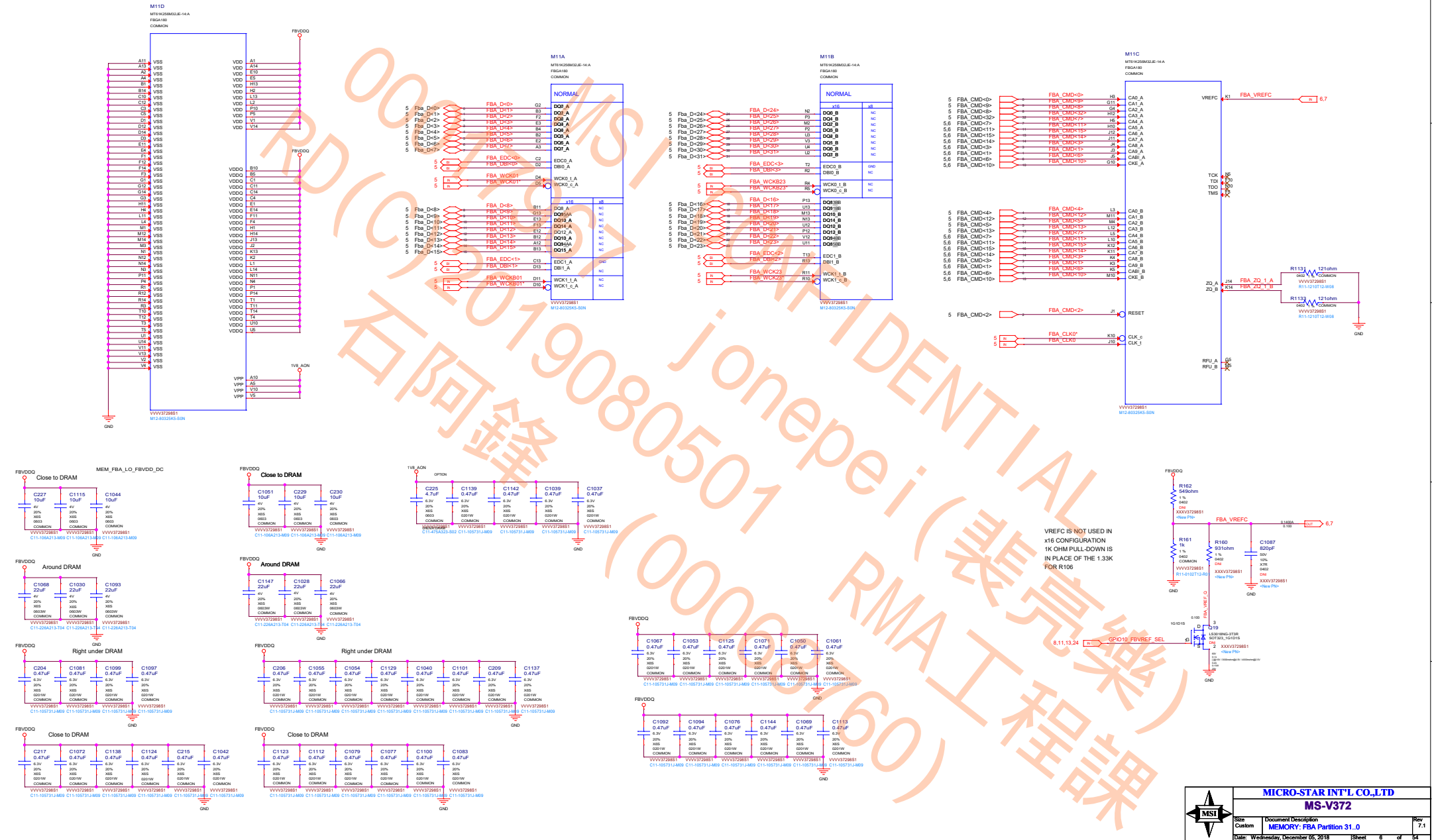
V372-3.2 change List
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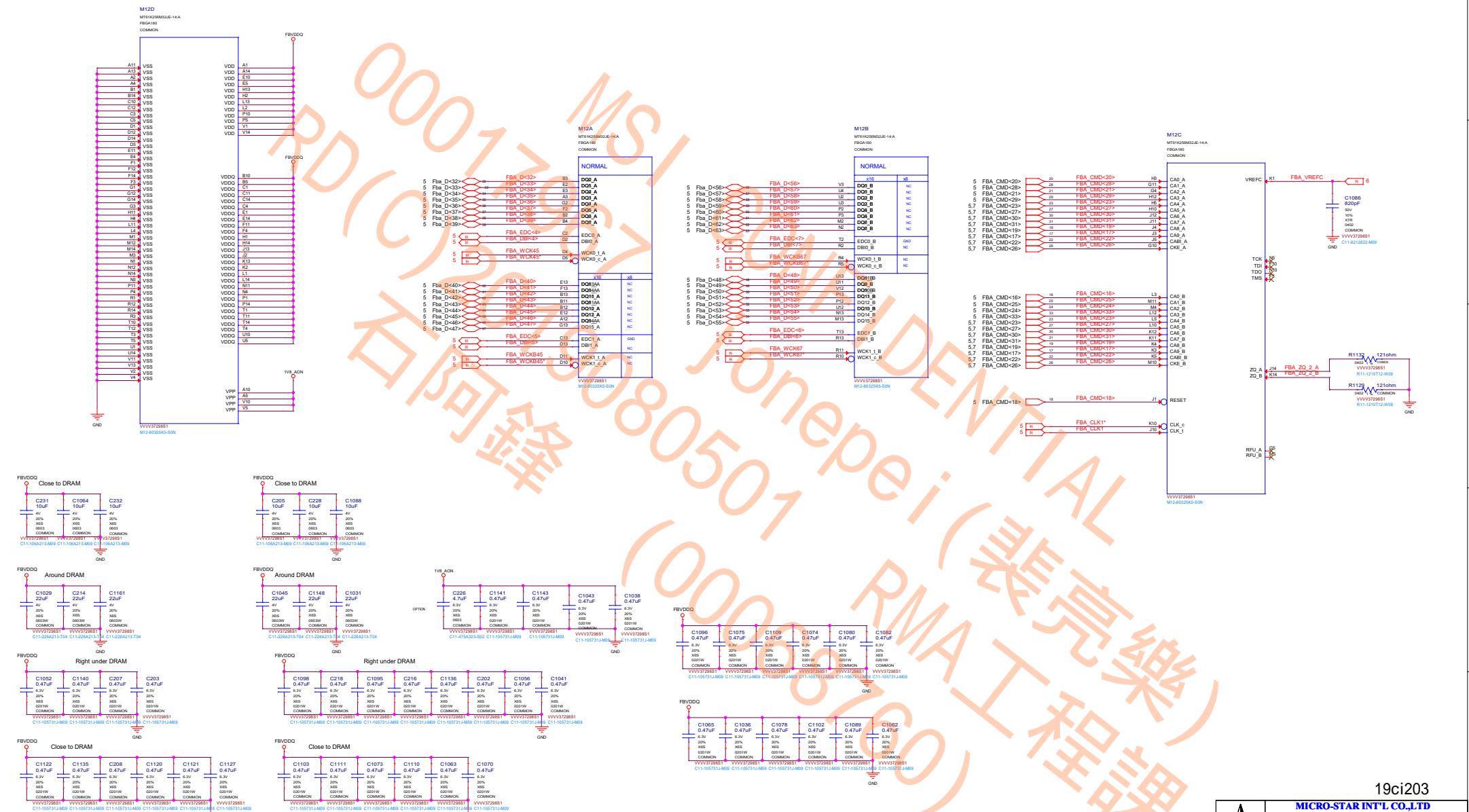
V372-3.0 change List
3 Remove I2CS · PEX_WAKE* · POWER_BRAKE* · 3V3_AUX_CON
19 Add DP_PWR bypass resistor
C12 changed to 560uF Solid CAP
22 Remove HDMI co-layout
C15 changed to 560uF Solid CAP
23 Remove SLI_BRG_PRST*
24 Remove POWER_BRAKE* · Unused GPIO
29 Add MP1475DJ for 5V Schematics
31 FBVDD controller changed to uP1666QQKF
33 FBVDD MO changed to UBIQ/QN3103M6N+QN3107M6N
34 NVVDD controller changed to MP2886A
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36 Remove NVVDD phase8-10
37 Remove some NVVDD output CAPs
39 Remove INPUT SWITCH RTD3
40 Remove INPUT SWITCH RTD3 USB
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43 Remove VR THERMAL PROTECTION
44 J8 changed to 6pin
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47 Remove GPIO1_GC6_FB_EN · 1V8MAIN ENABLE
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44 Remove SLI_BRG_PRST* · PS_1V8_AON_EN · THERM_OVERT*
Remove PS_SLI_FGC6_OR · PS_FBVDD_BUFF_R
49 Remove GPIO1_GC6_FB_EN · PS_RTD3_12V_SW
Remove 12V Voltage Monitor
51 Remove PEX_WAKE
53 Remove LED_CONTROLLER_IT8295

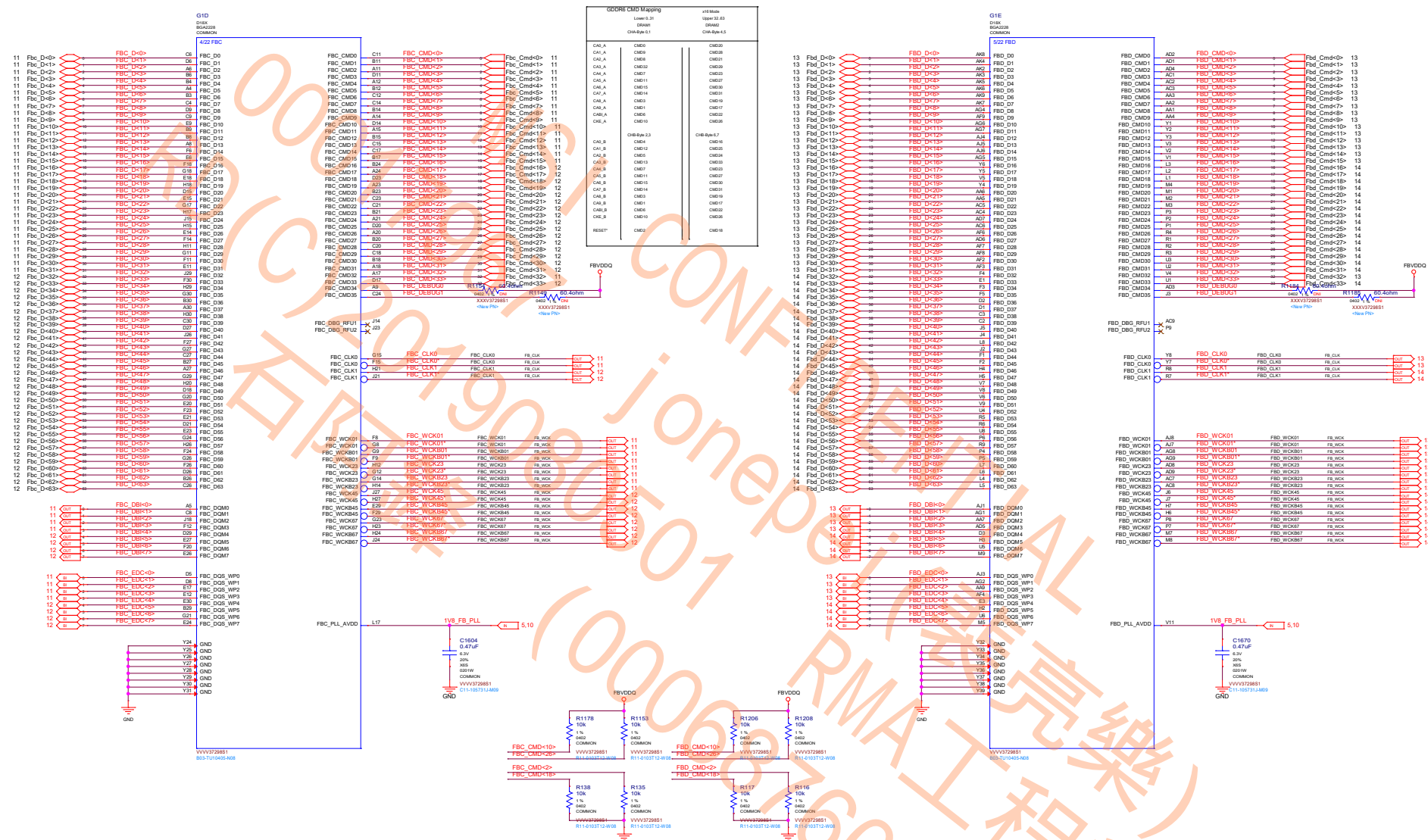


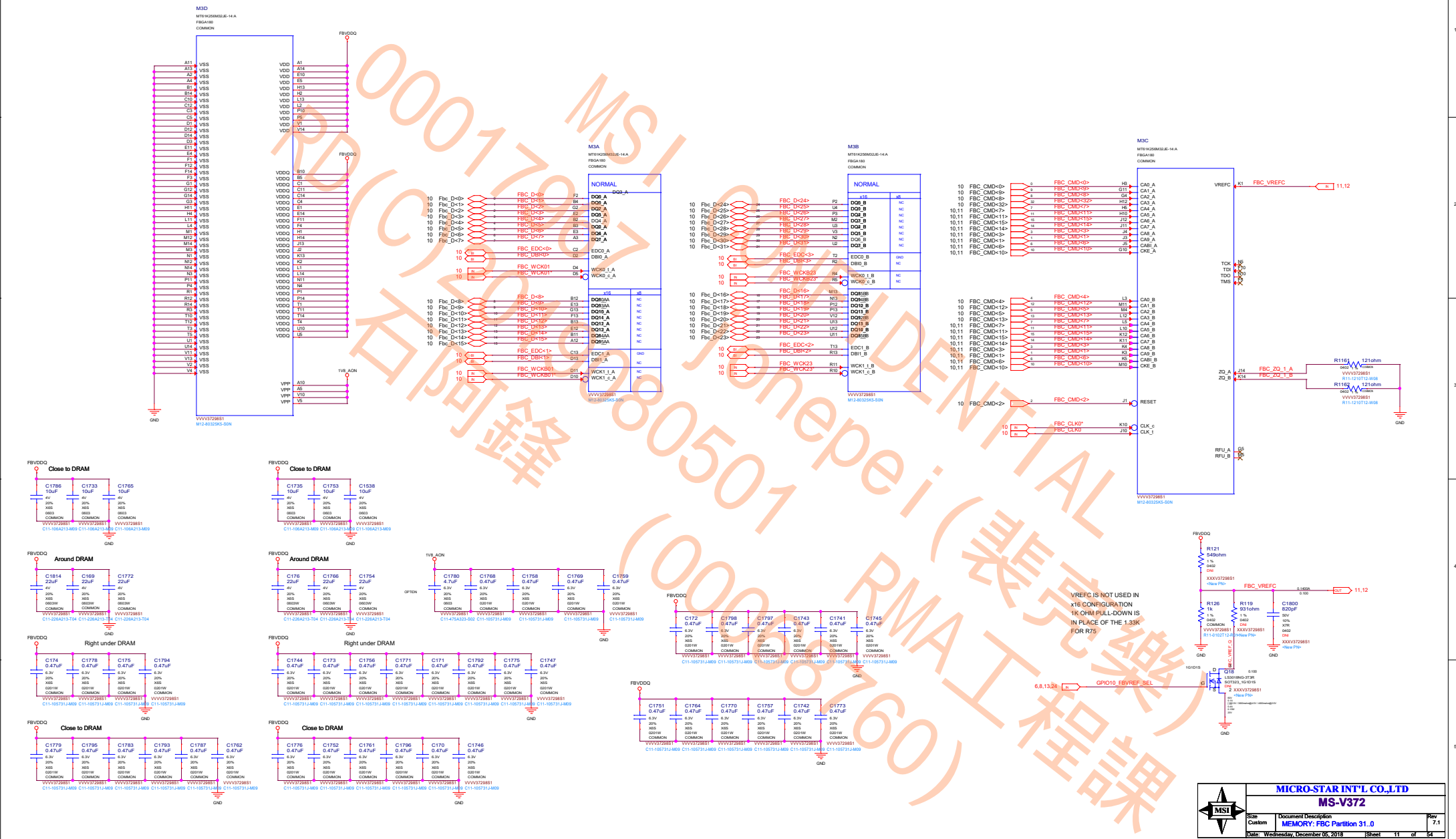


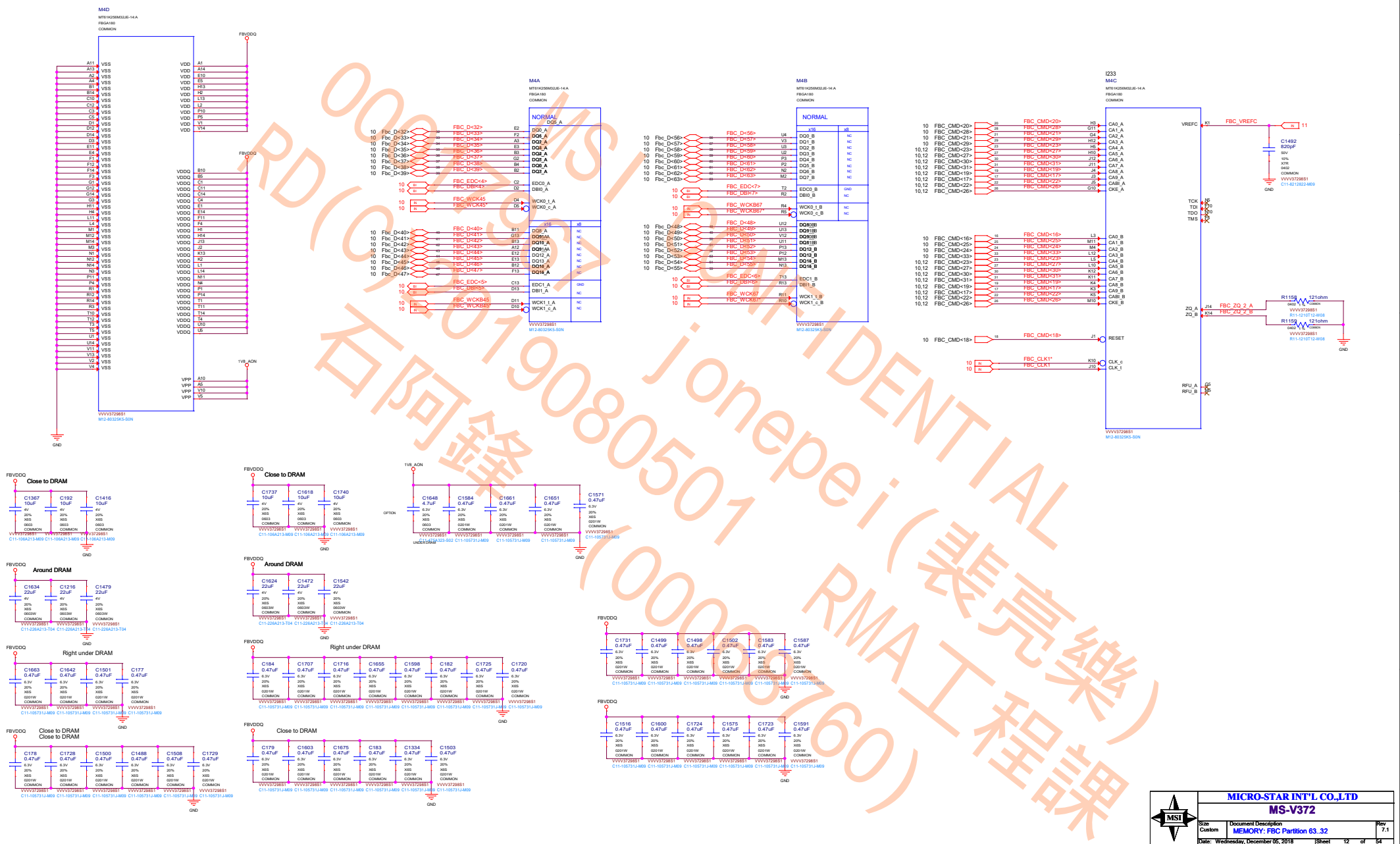








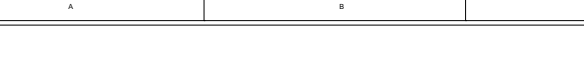
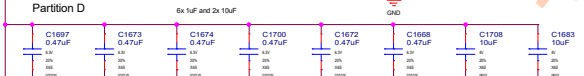
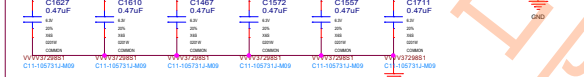
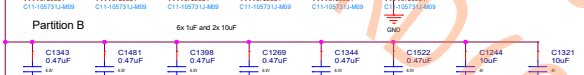
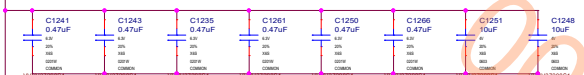




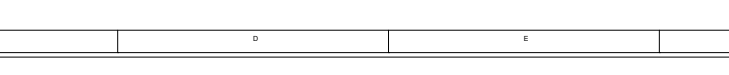
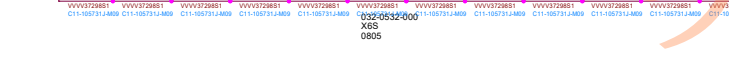
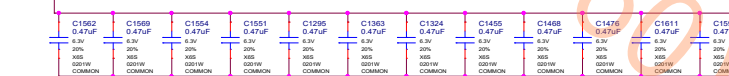
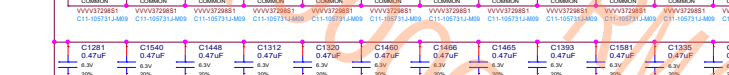
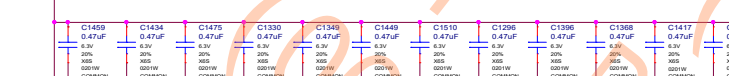
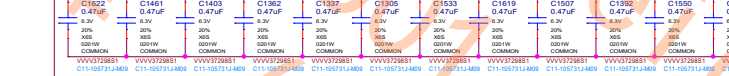
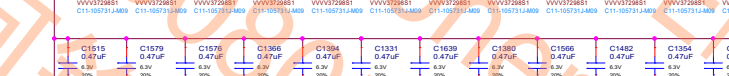
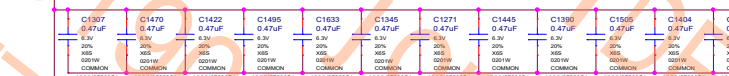
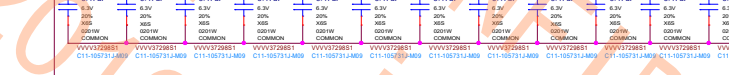
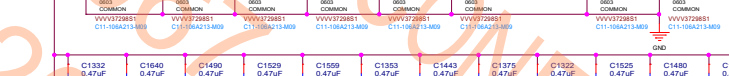
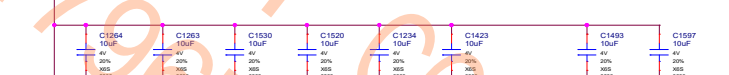
NVVDD

FBVDDQ

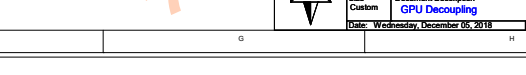
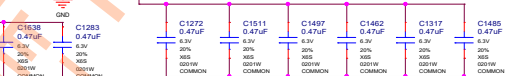
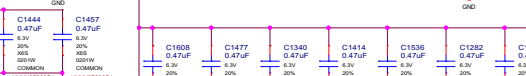
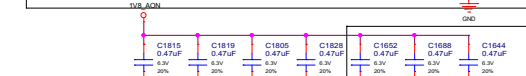
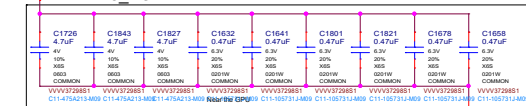
Partition A



NVVDD



1V8 AON



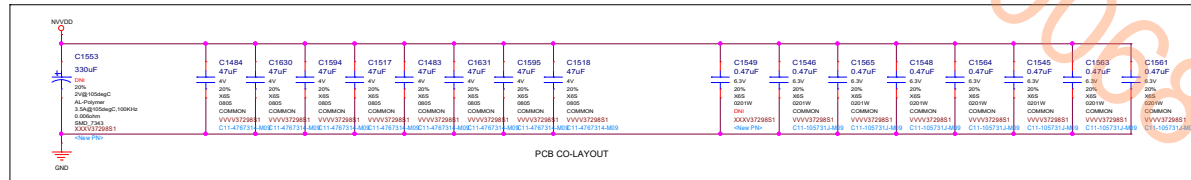
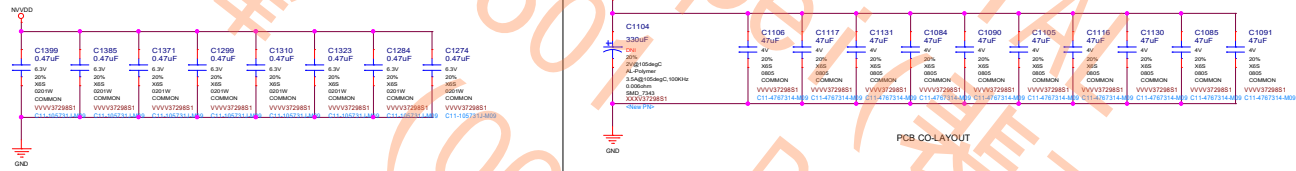
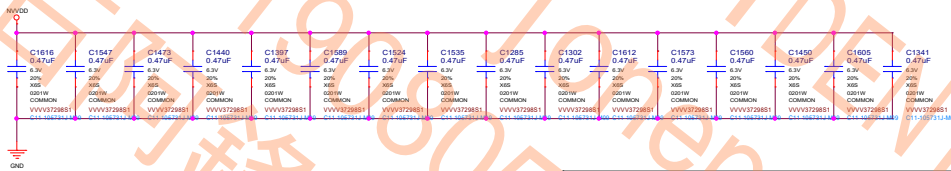
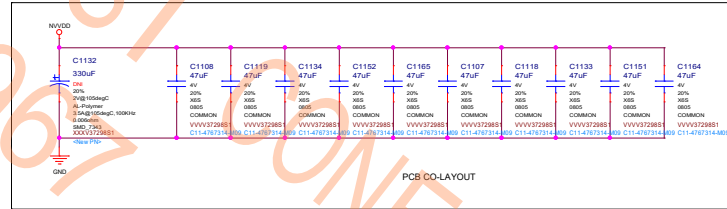
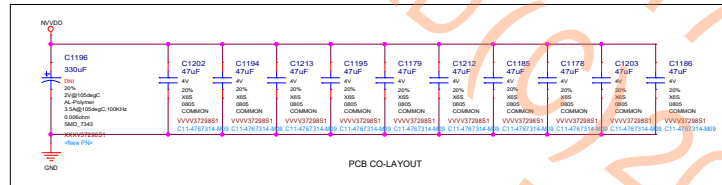
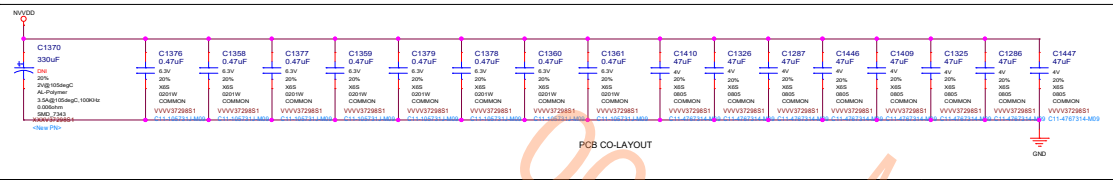
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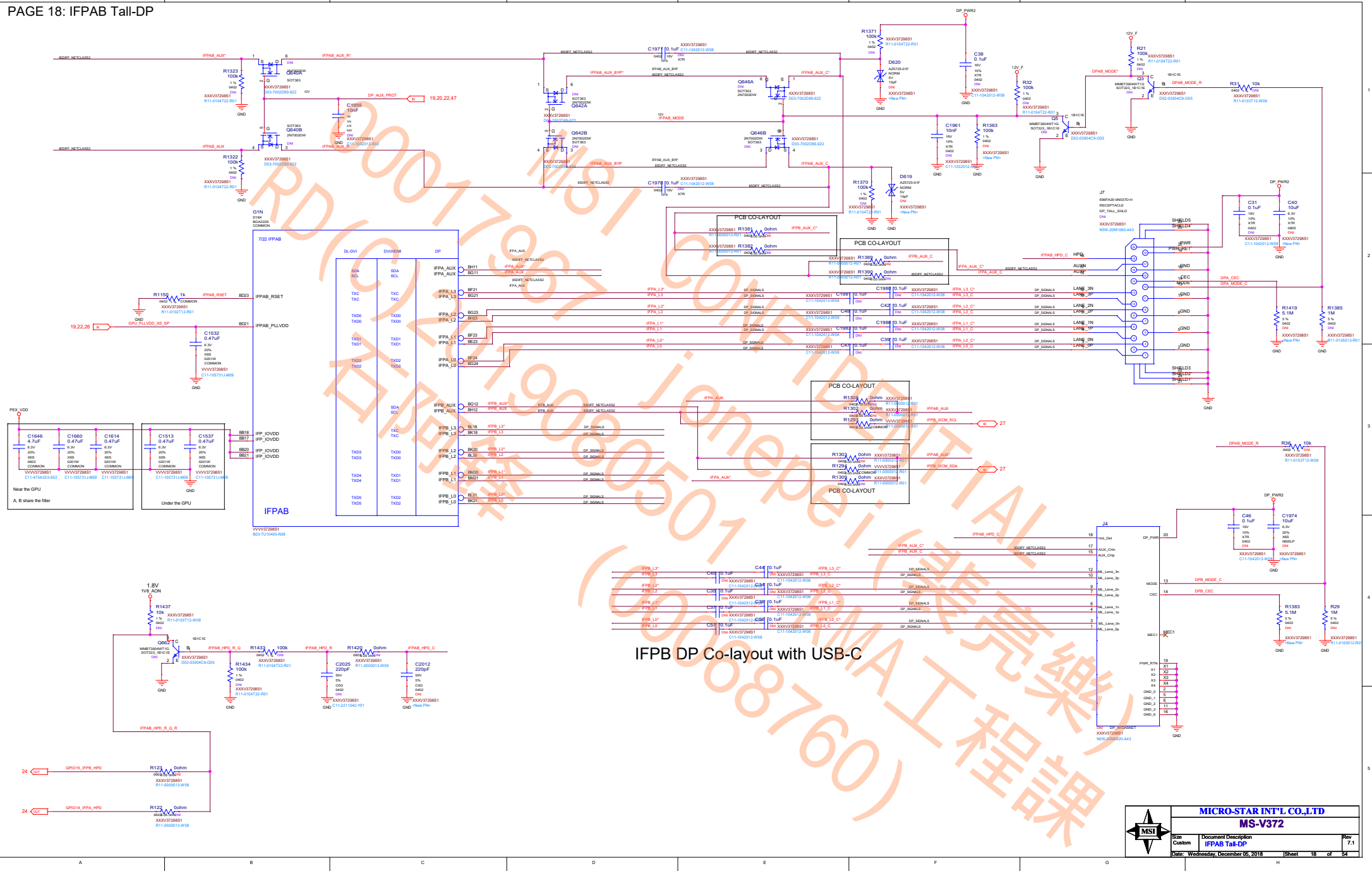
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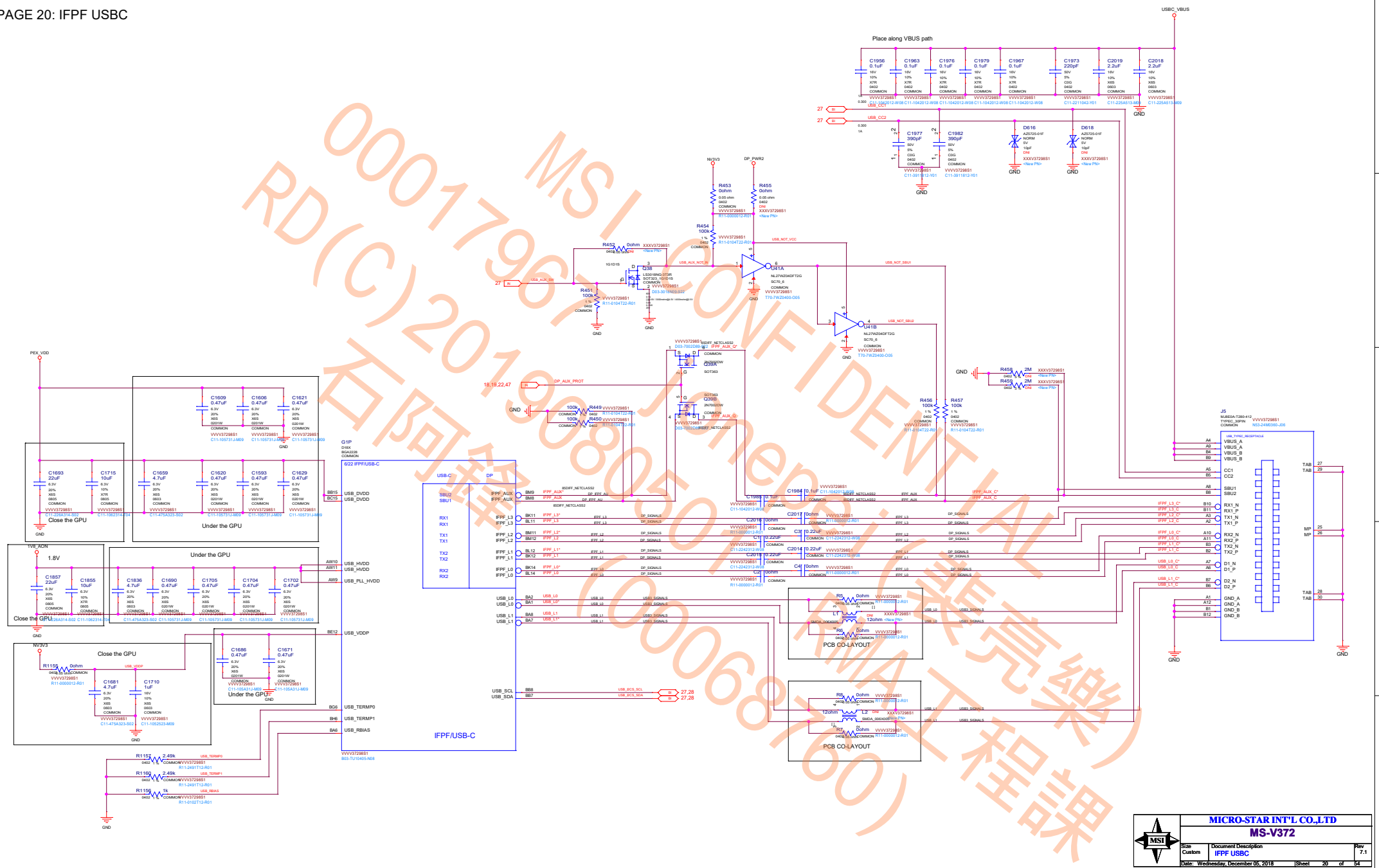


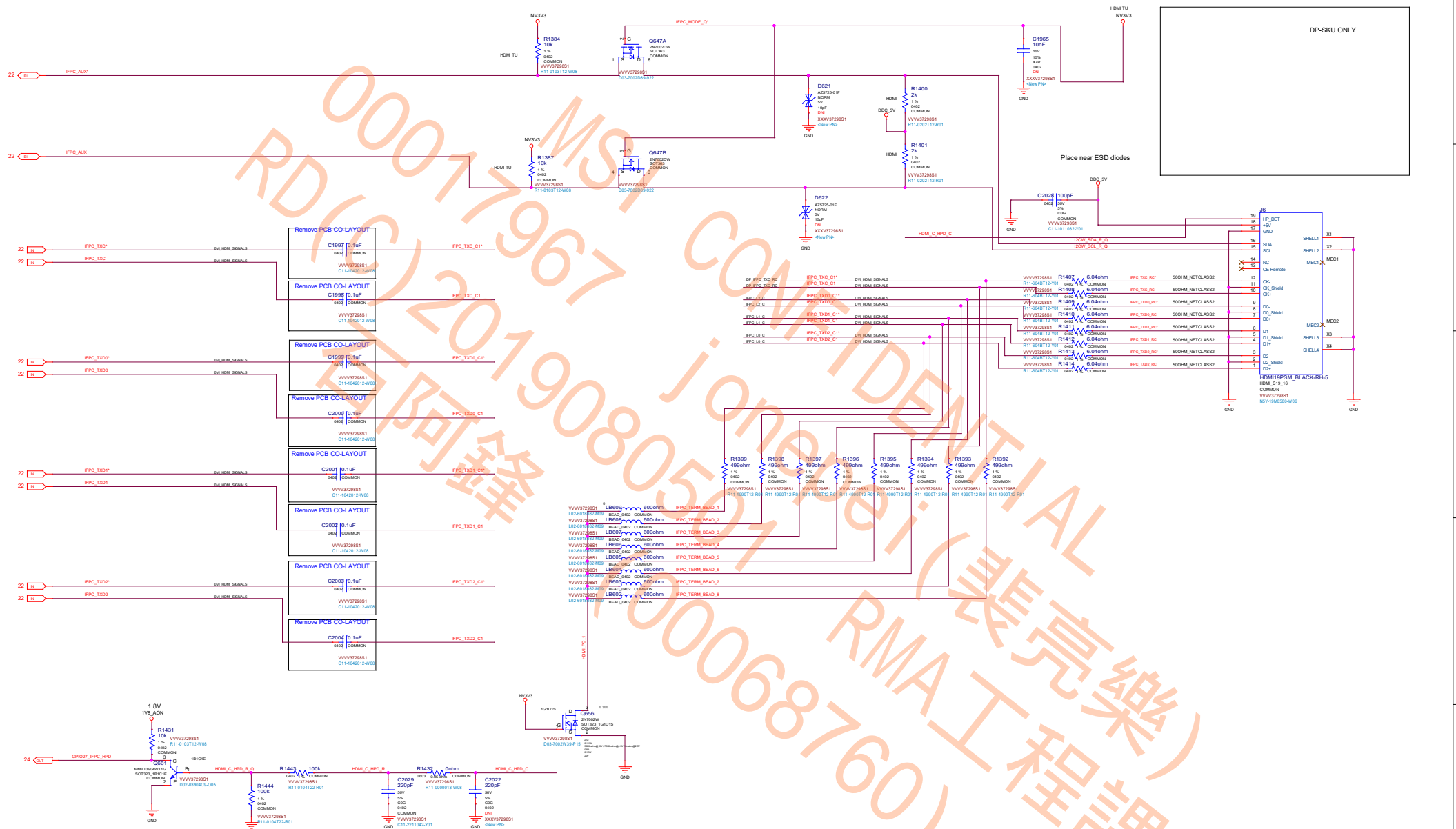
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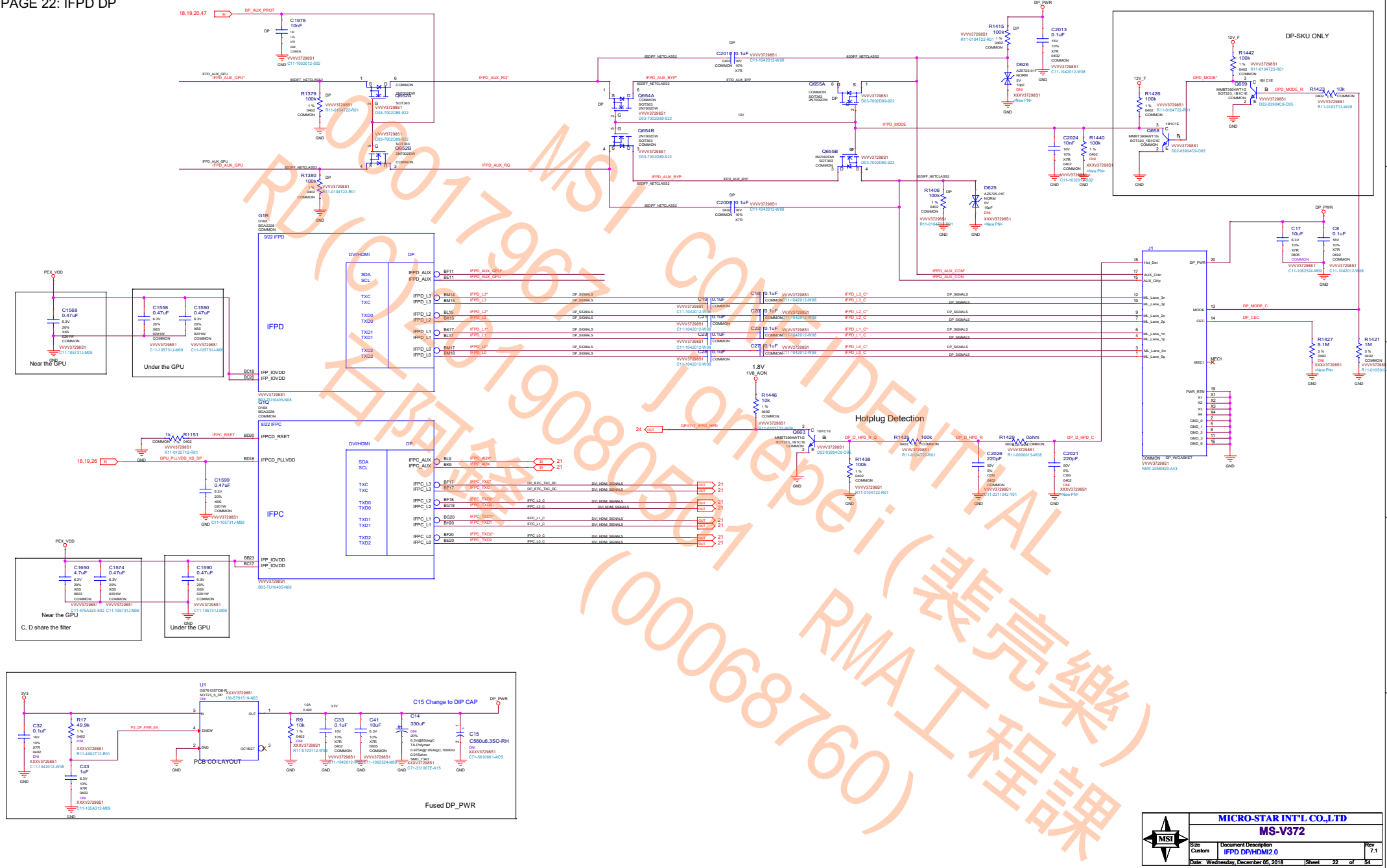
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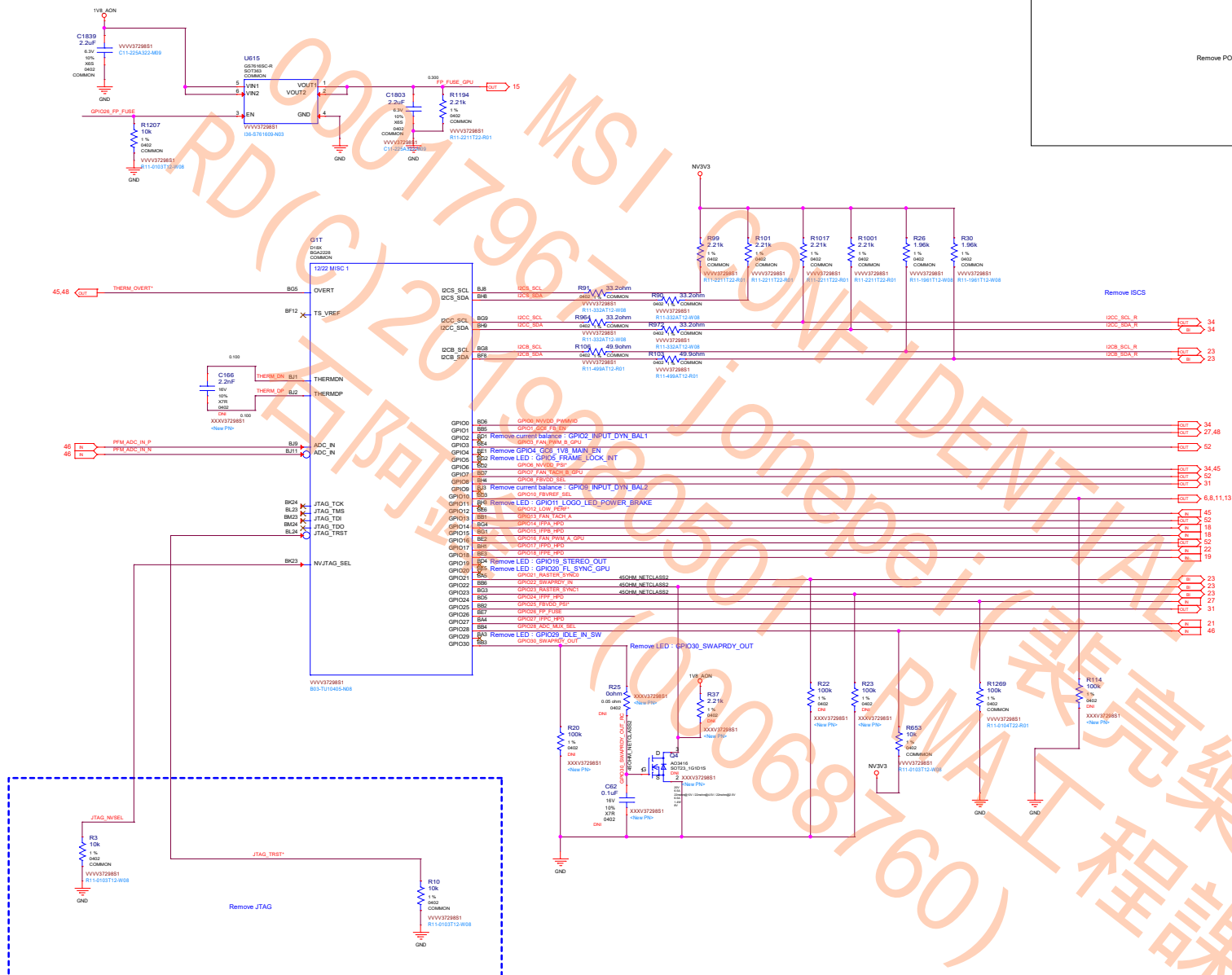
Size	Document Description	Rev
Custom	GPU Decoupling	7.1
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Remove POWER_BRAKE*

[Remove ISCS](#)

I2CB_SCL_R





H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	
L	L	L	XXX1	1:ENABLE 0:DISABLE FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

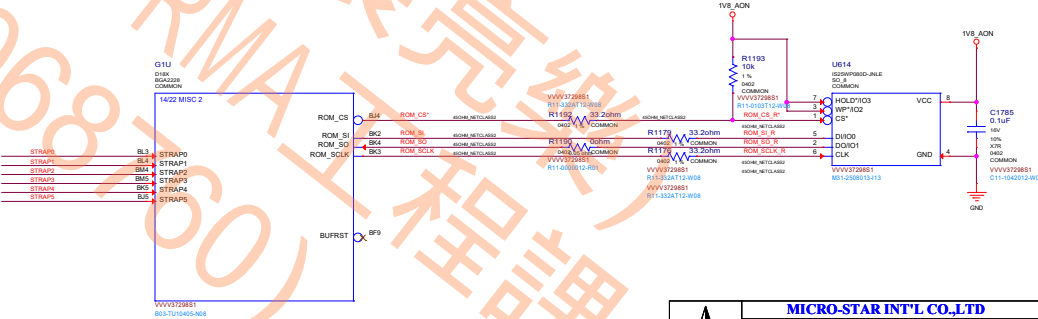
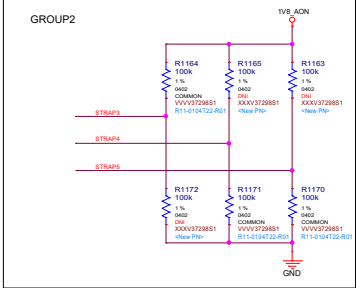
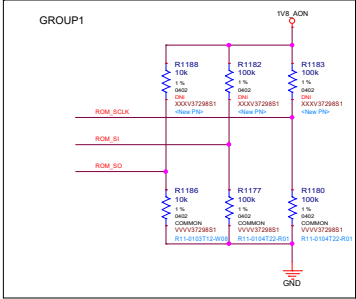
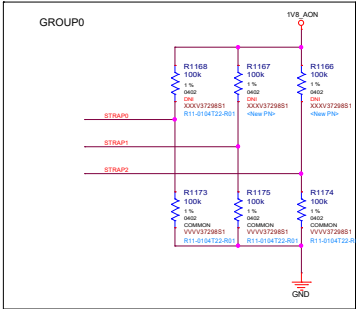
DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	

- 1:SMB_ALT_ADDR ENABLE
- 0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
- 0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
- 0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
- 0:VGA_DEVICE DISABLE

Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung





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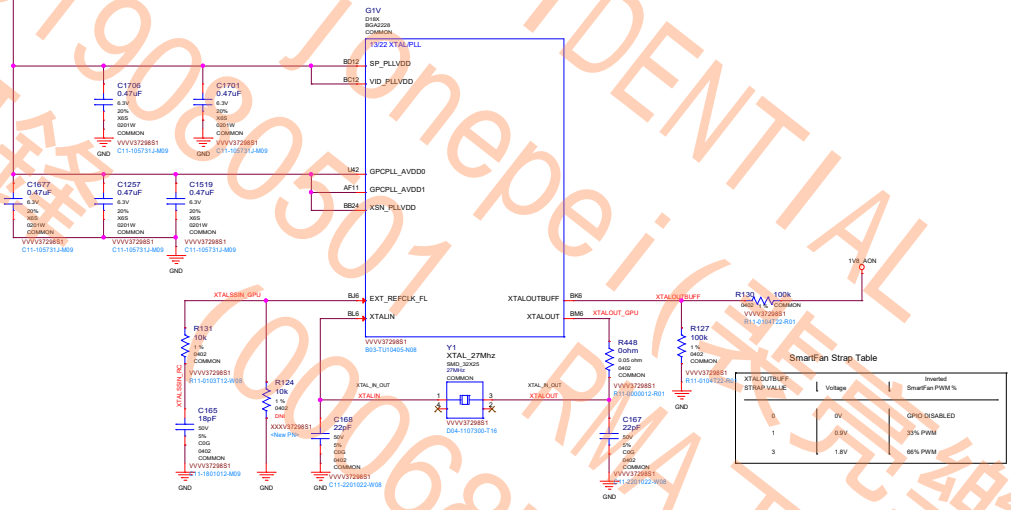
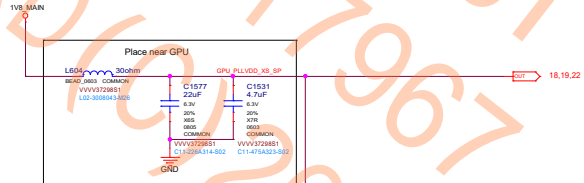
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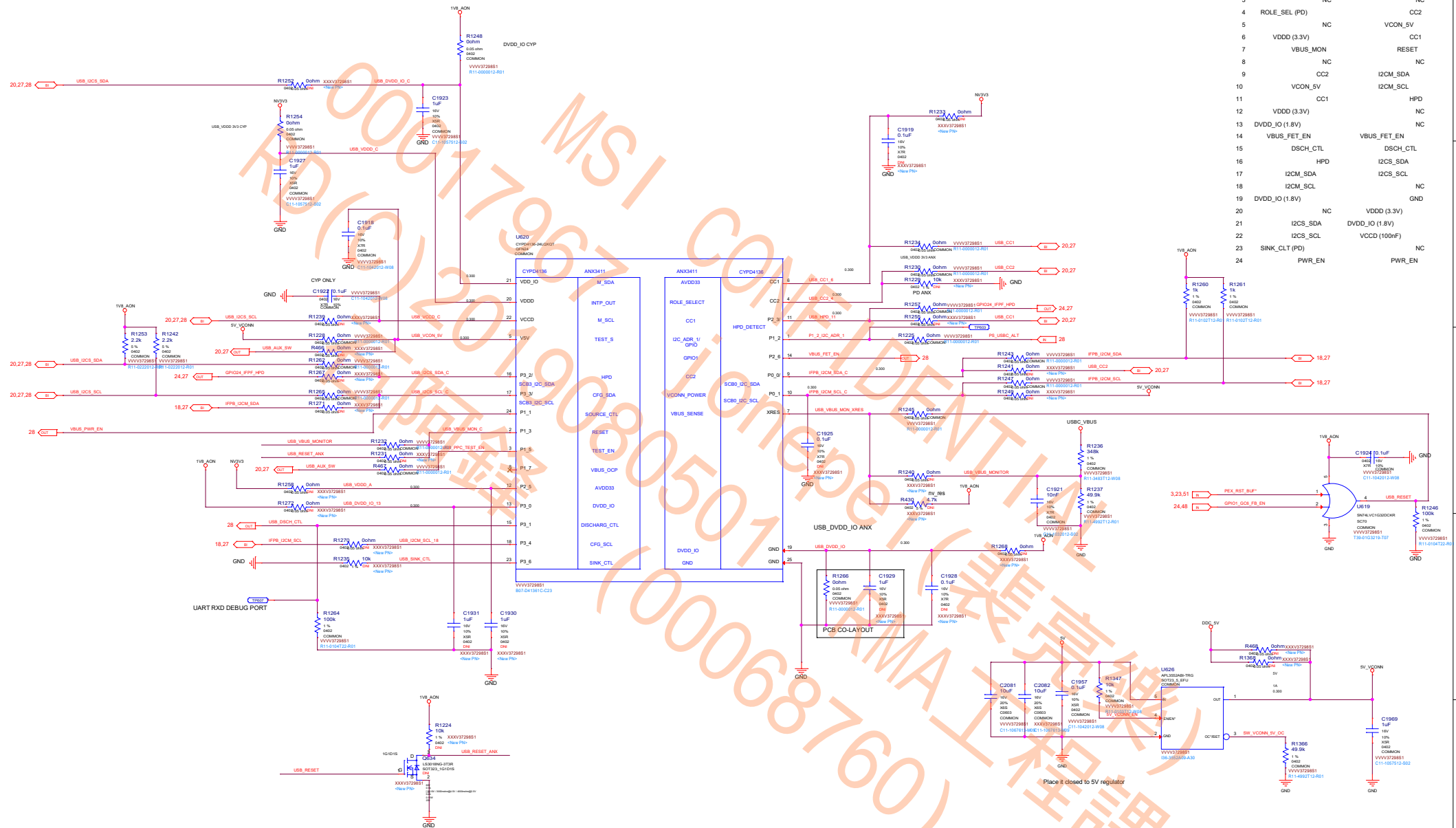
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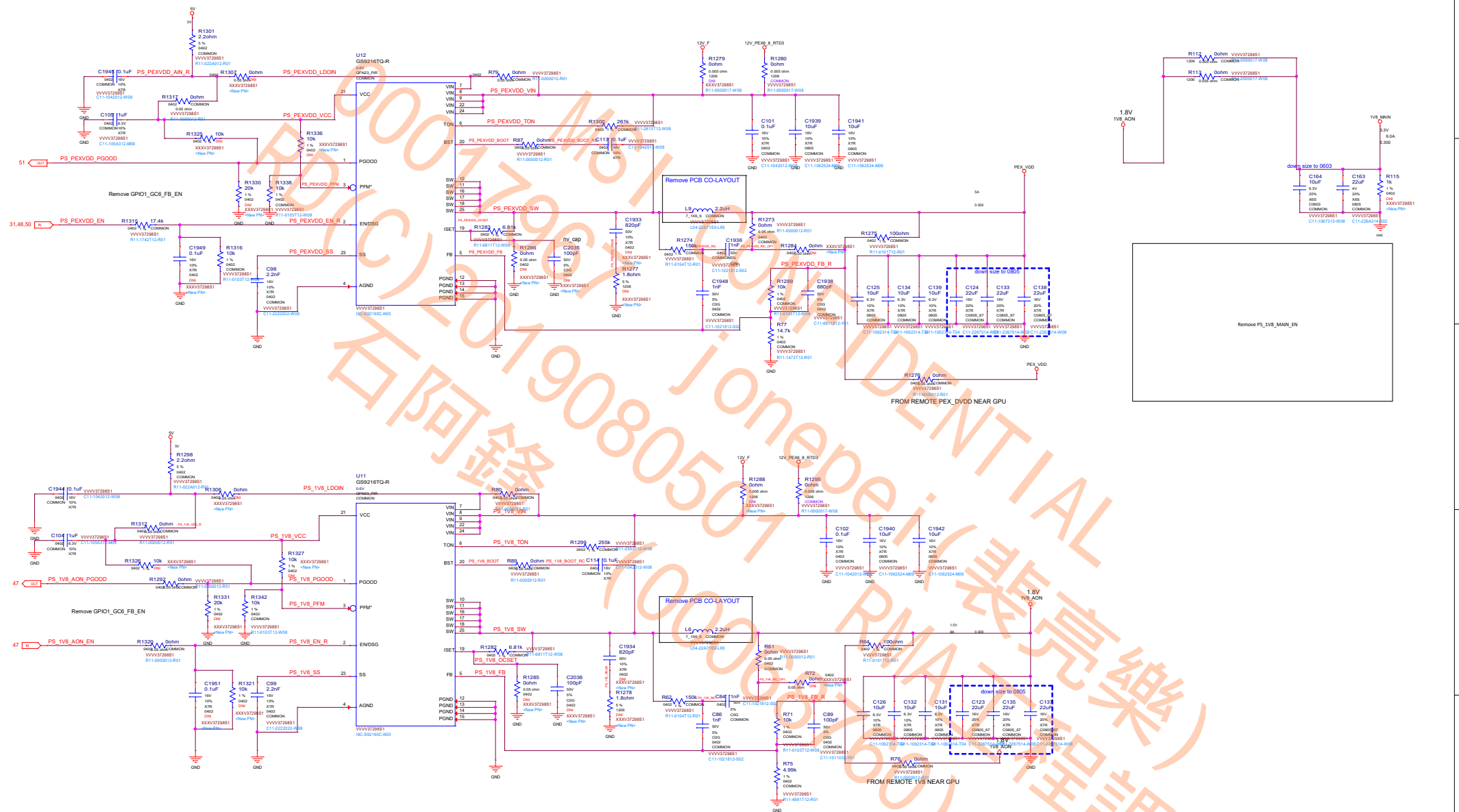


SmartFan Strap Table

STRAP VALUE	Voltage	Inverted SmartFan PWM %
1	0V	GPIO DISABLED
2	0.5V	35% PWM
3	1.0V	65% PWM



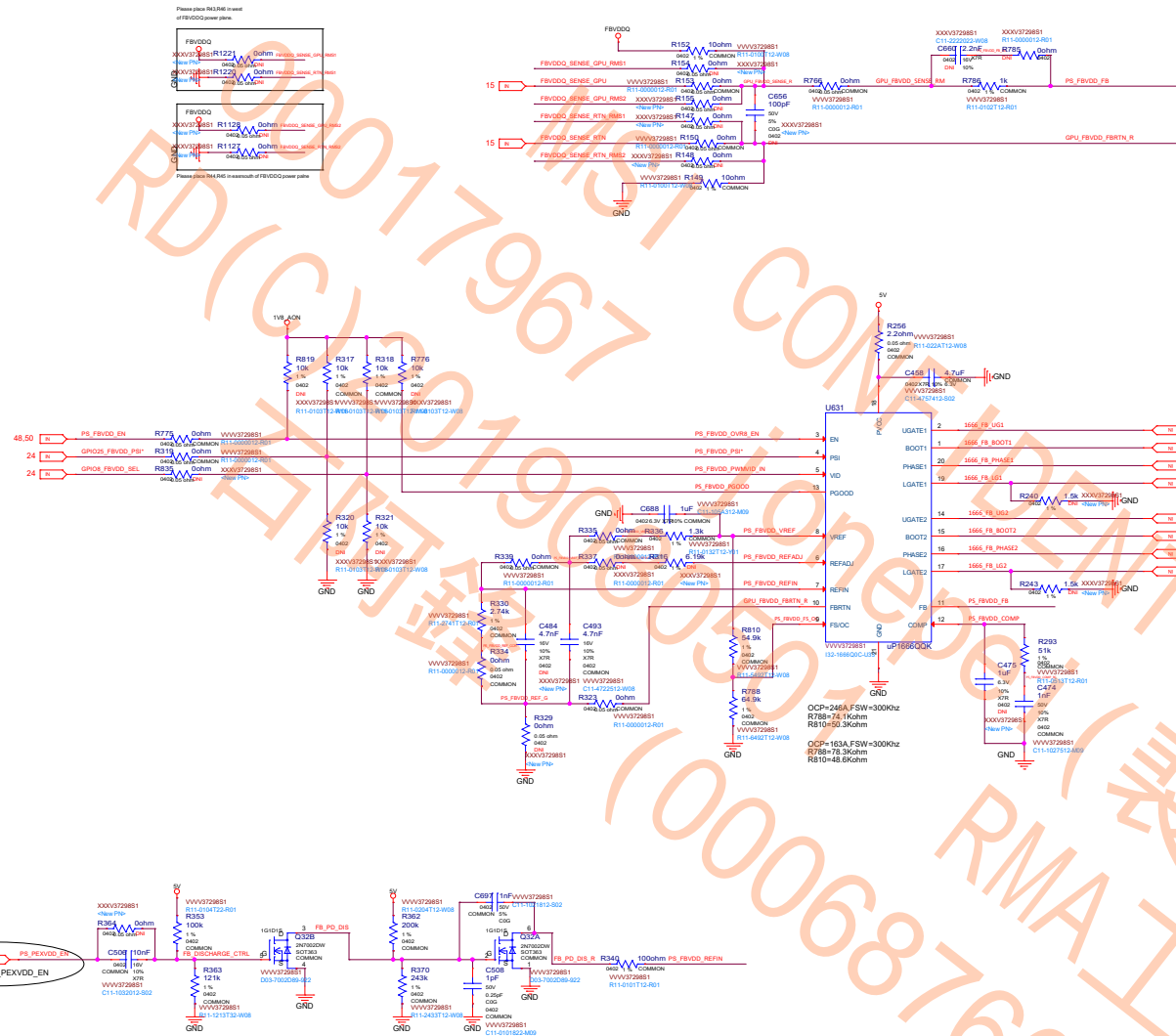
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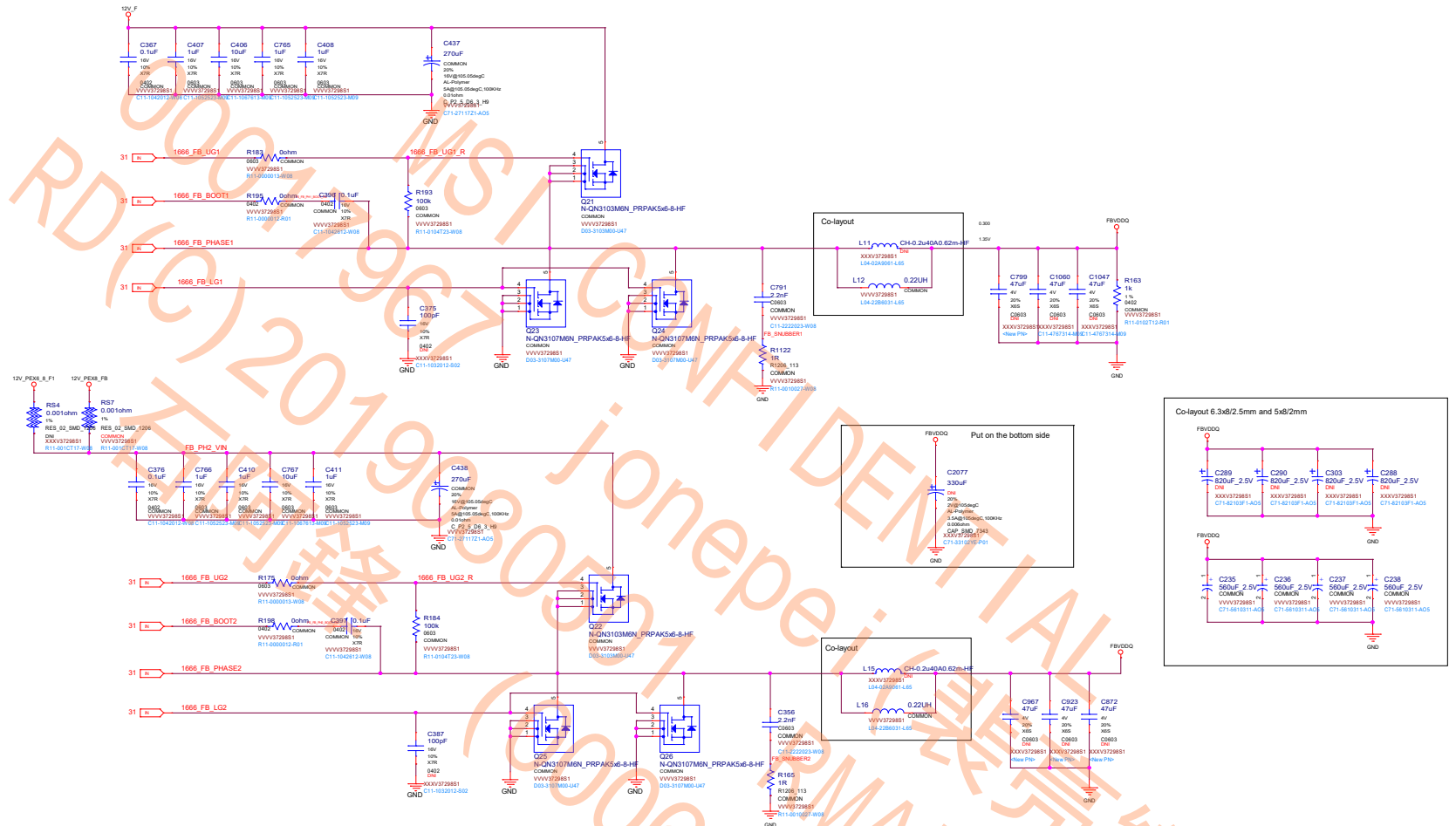


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RD(C)2019080501 RMA工程課
石阿鋒 (00068760)

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	MS-V372		
	Size	Document Description	Rev
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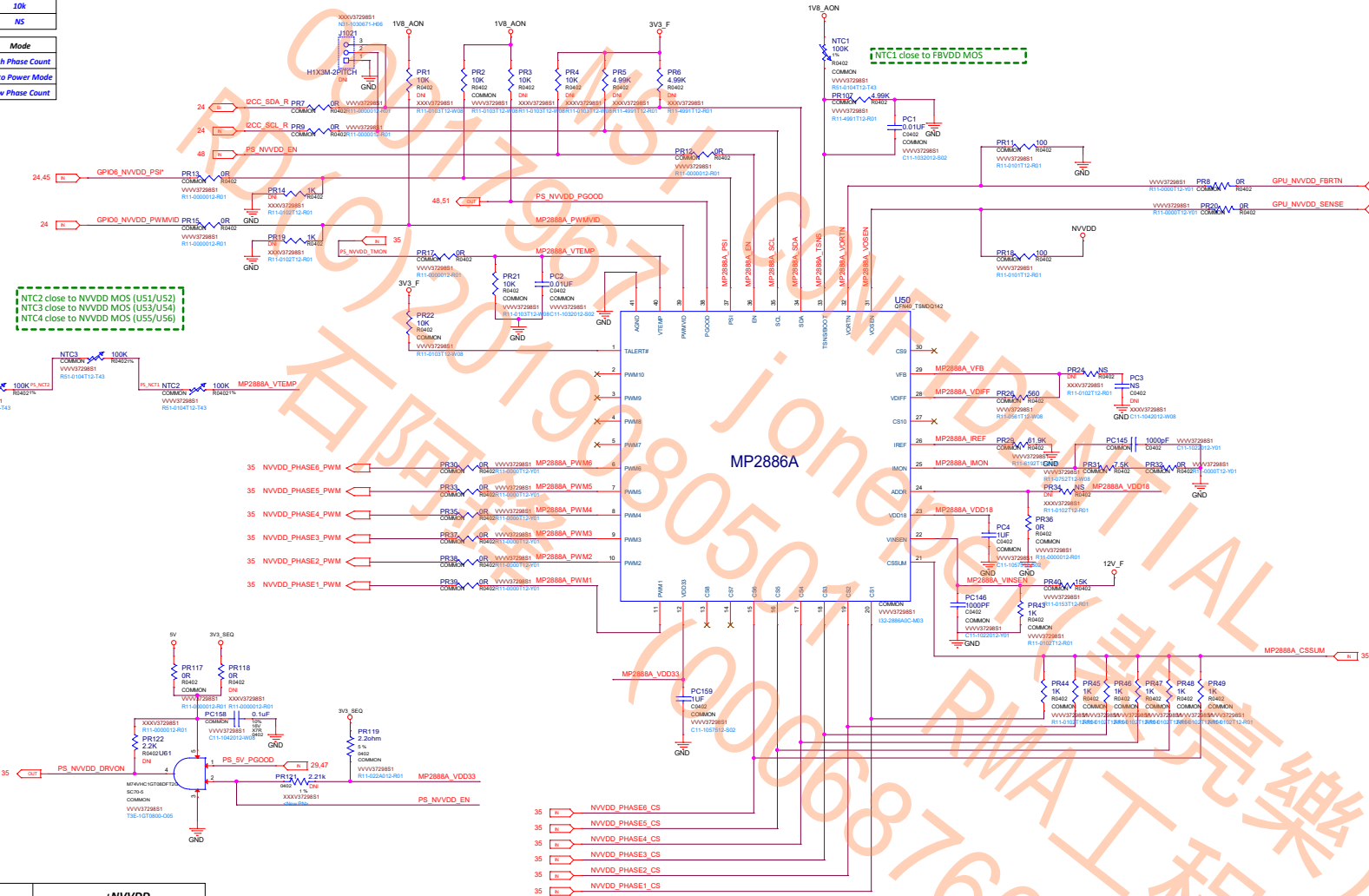
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EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

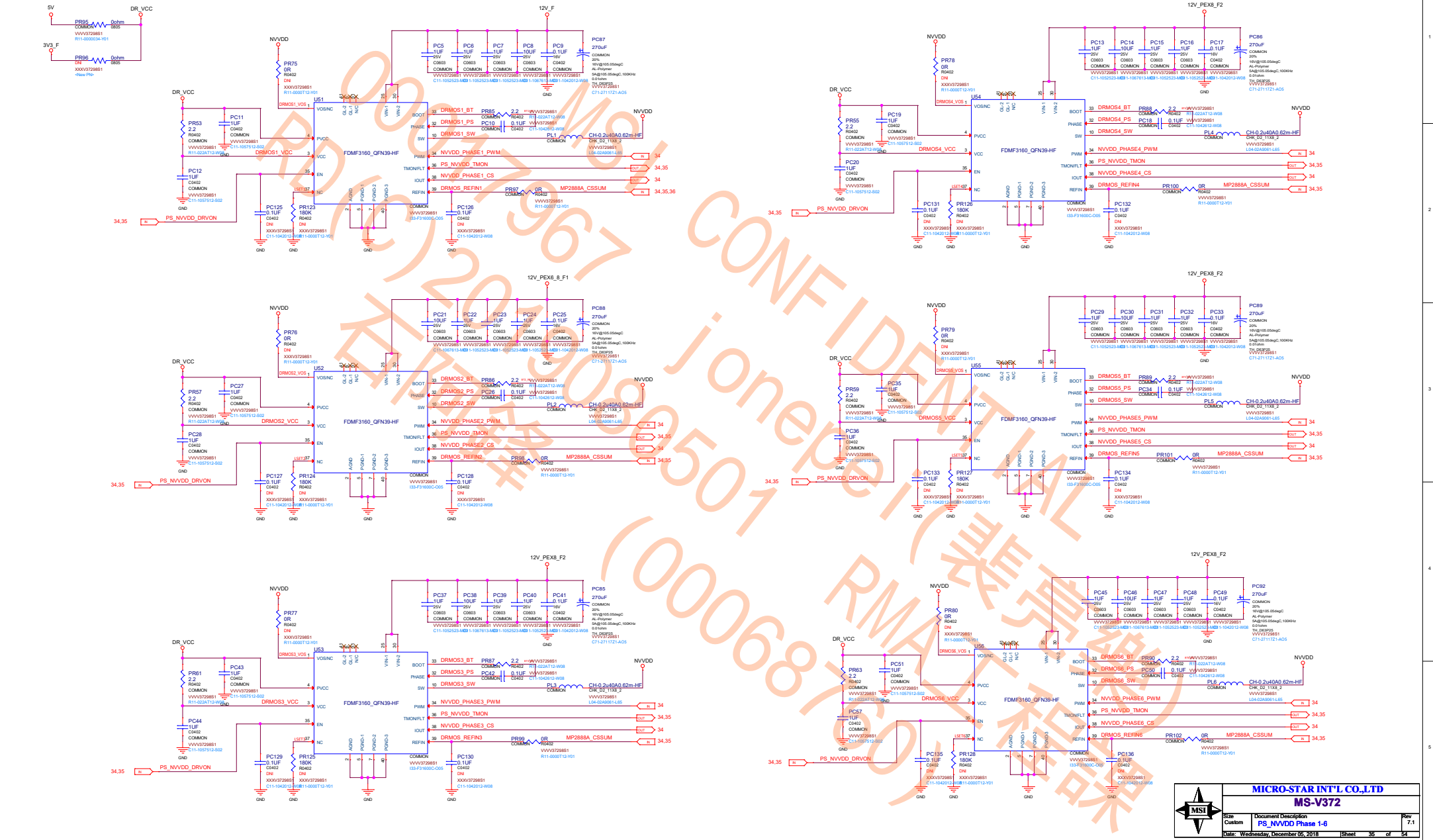
PWMVDD	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1fh




	+NVVDD
TDC	200A
IccMax	330A
Vboot	0.8V
Load Line	0mohm

PMBus Address	Setting Point(V)	Rmax (kΩ) 1%	Rmax (kΩ) 1%
20h	0	-	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

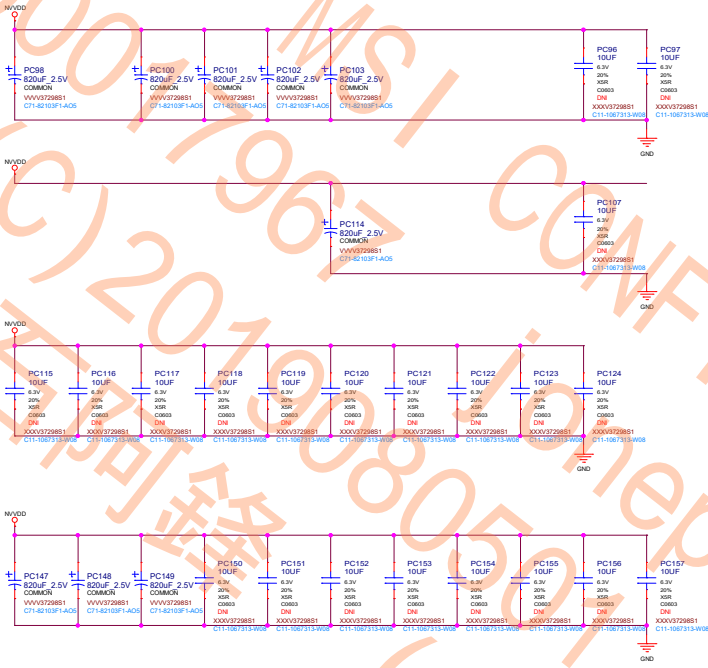
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MS-V372			
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Custom	PS: NVVDD Controller	7.1	
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	MICRO-STAR INT'L CO.,LTD	
	MS-V372	
	Size	Rev
	Custom	7.1
Document Description		
PS: NVVDD Phase(X)		
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NVVDD Output CAP

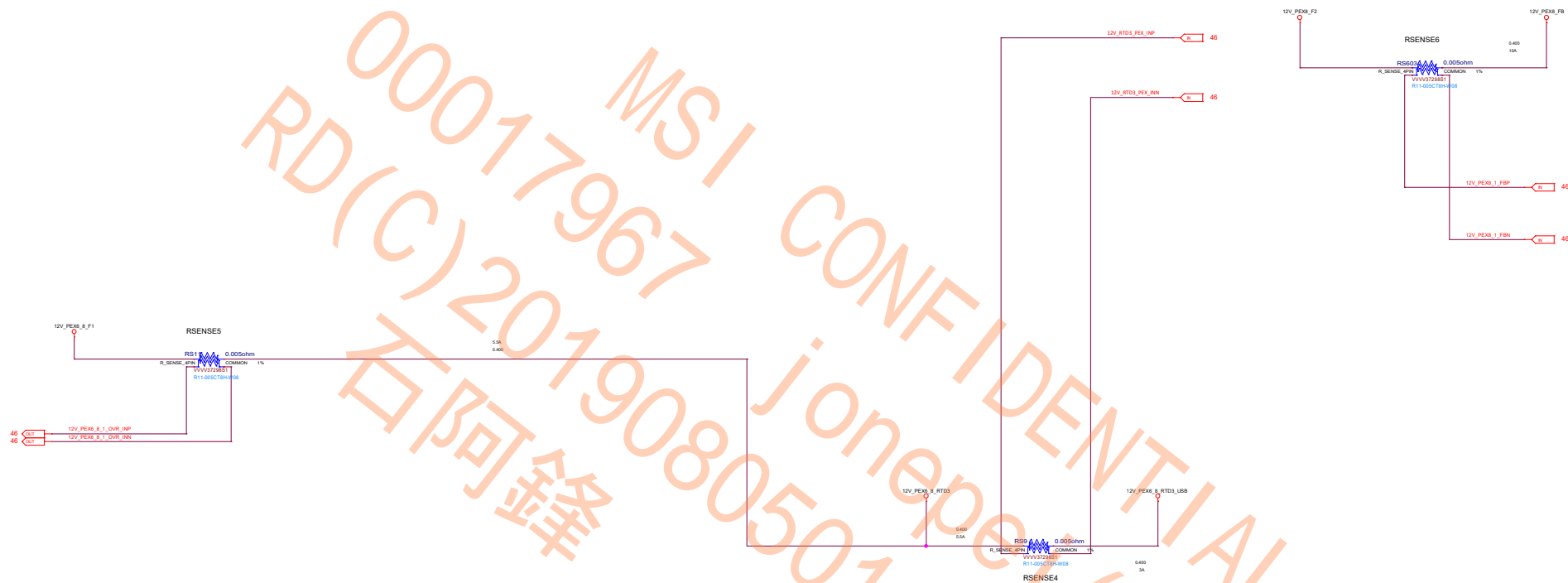


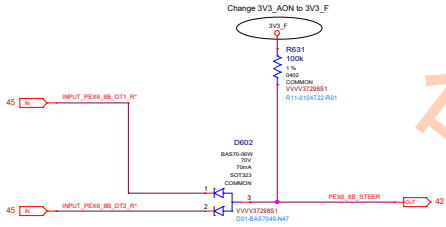
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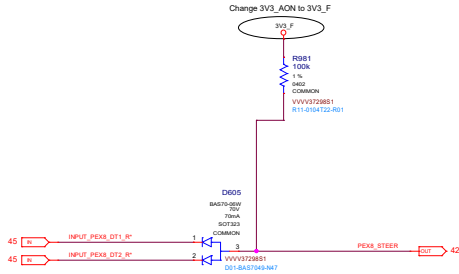
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Size	Document Description	Rev
Custom	PS: INPUT SWITCH RTD3	7.1
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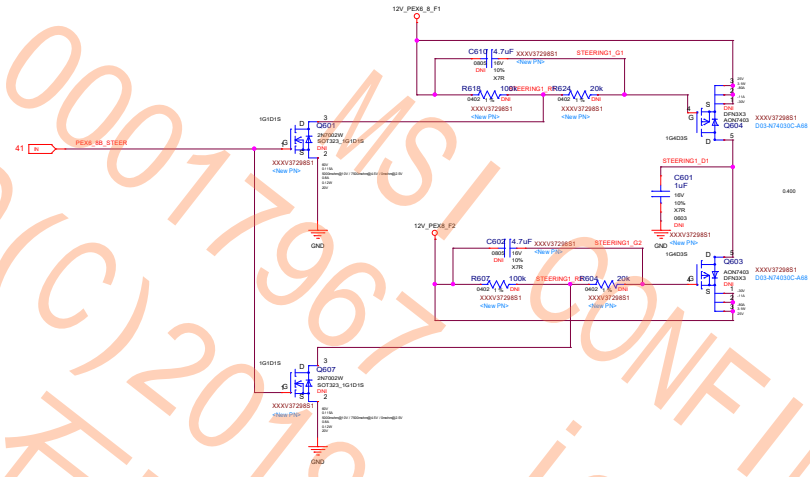




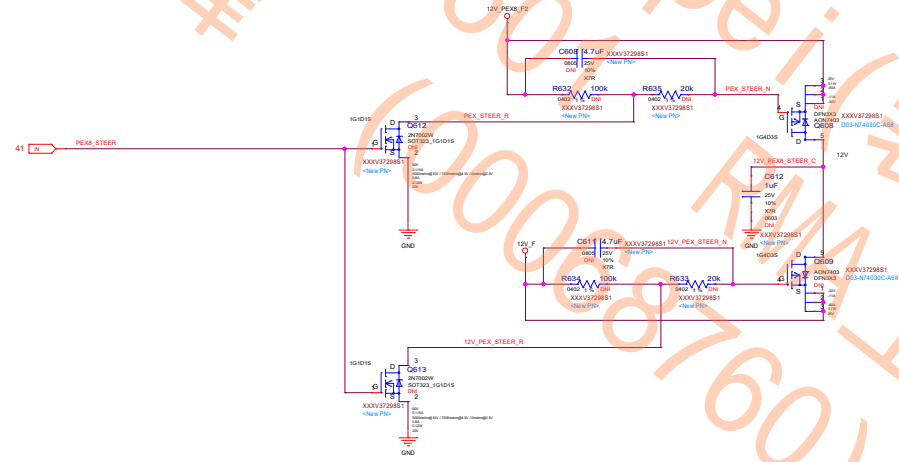
Remove 3V3_F bypass to 3V3_AON



12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

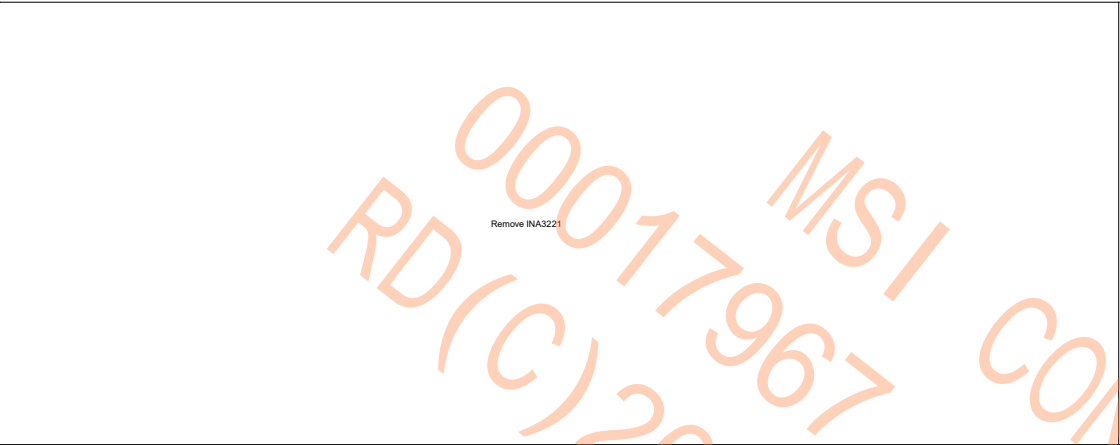


12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

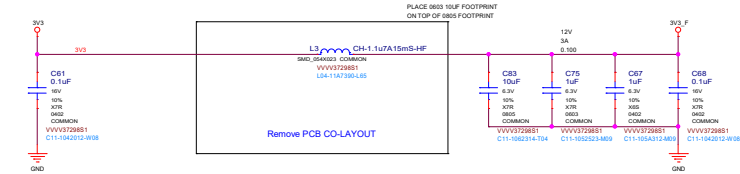


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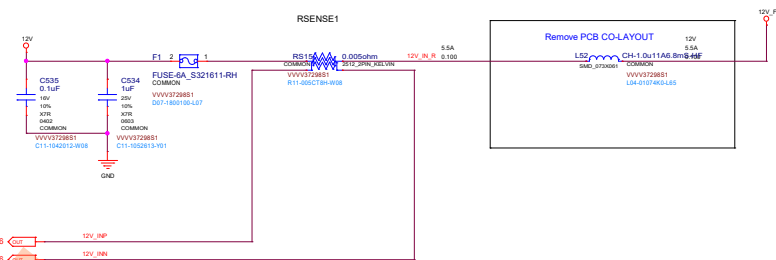
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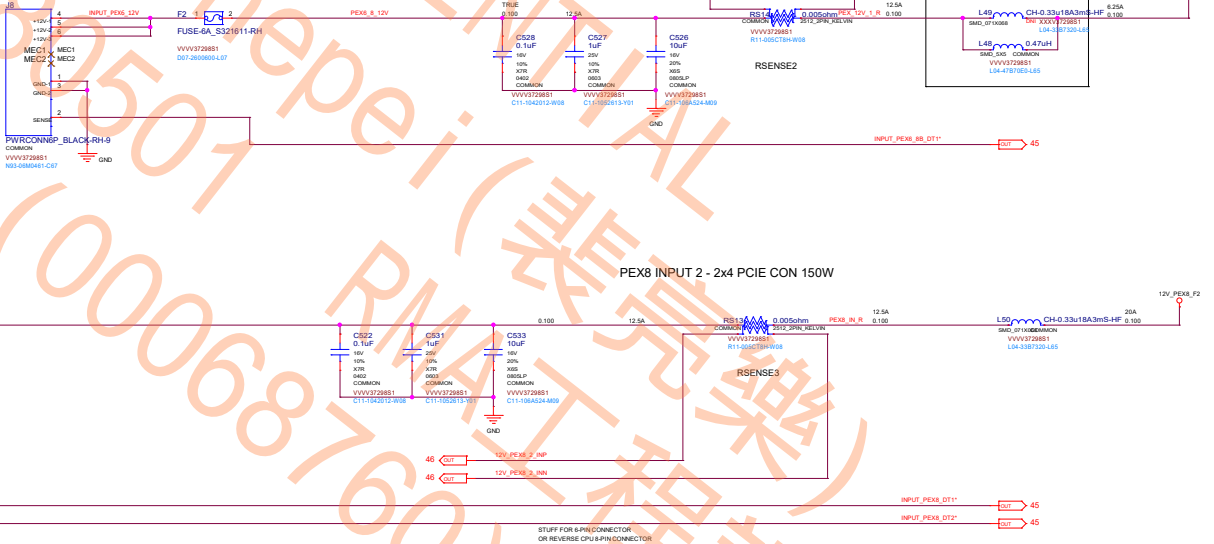
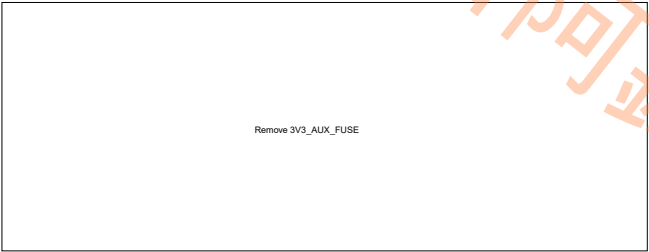
PEX 3V3 INPUT - 10W



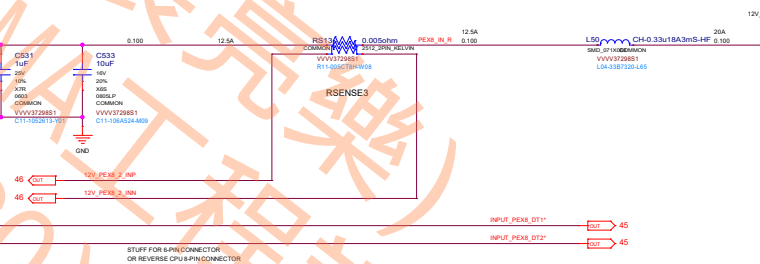
PEX_12V INPUT - 66W



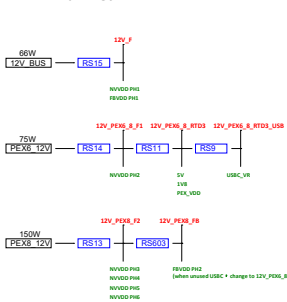
PEX6 INPUT 1 - 2x3 PCIE CON 75W

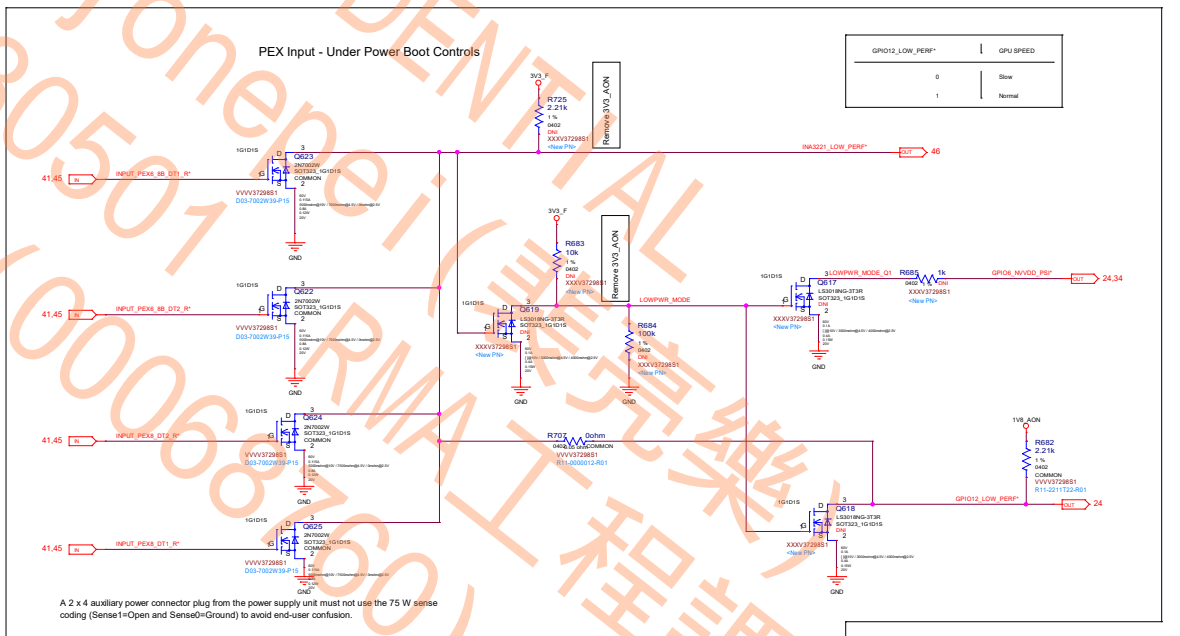
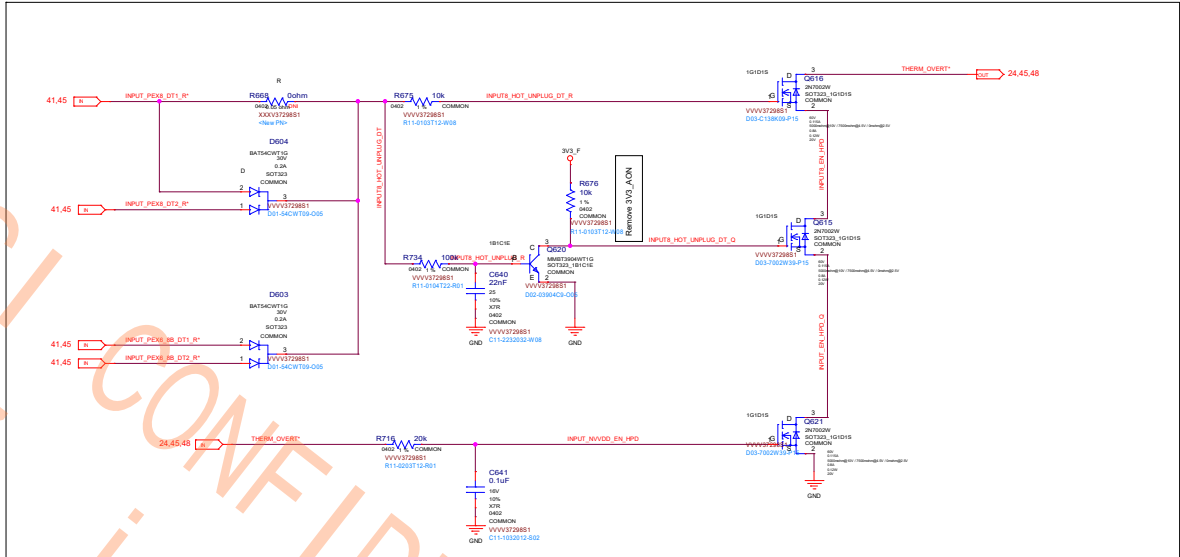
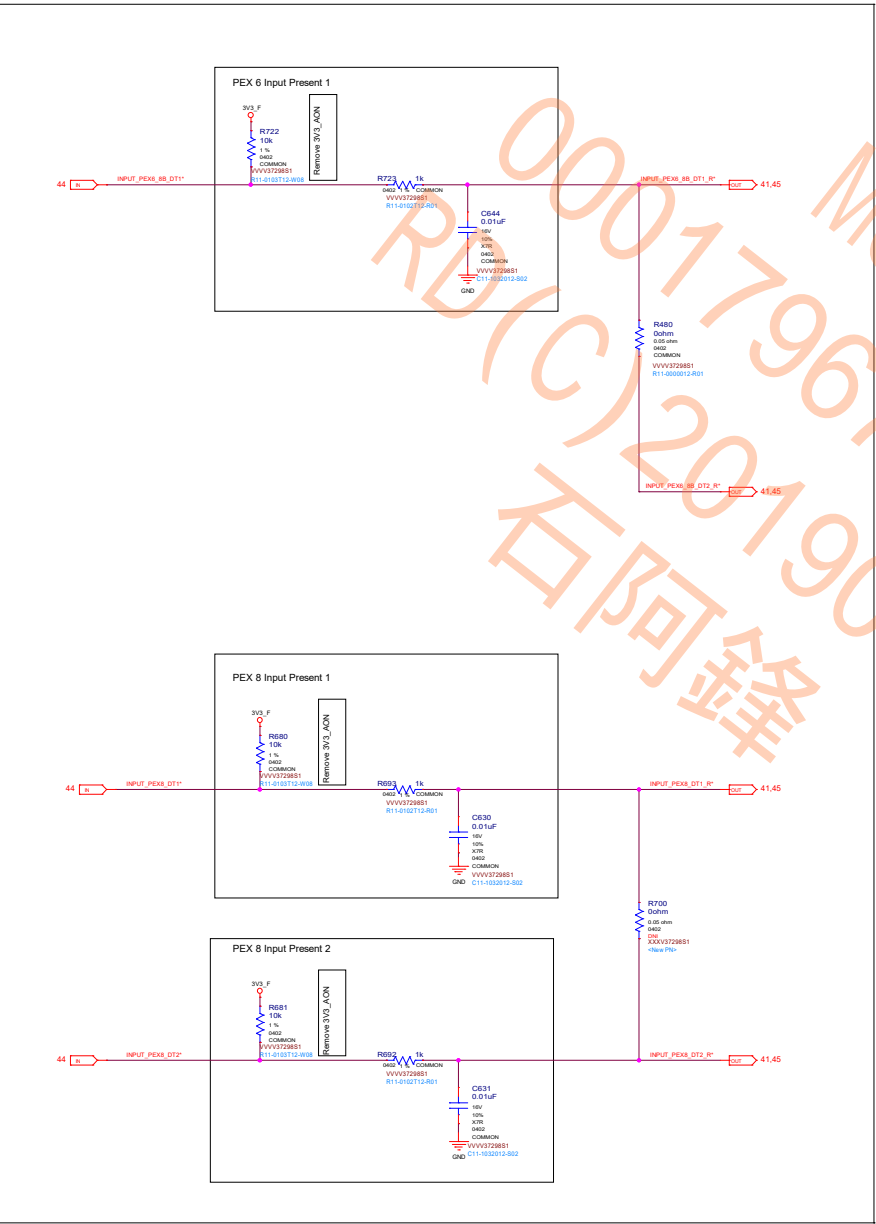


PEX8 INPUT 2 - 2x4 PCIE CON 150W



Power Topology

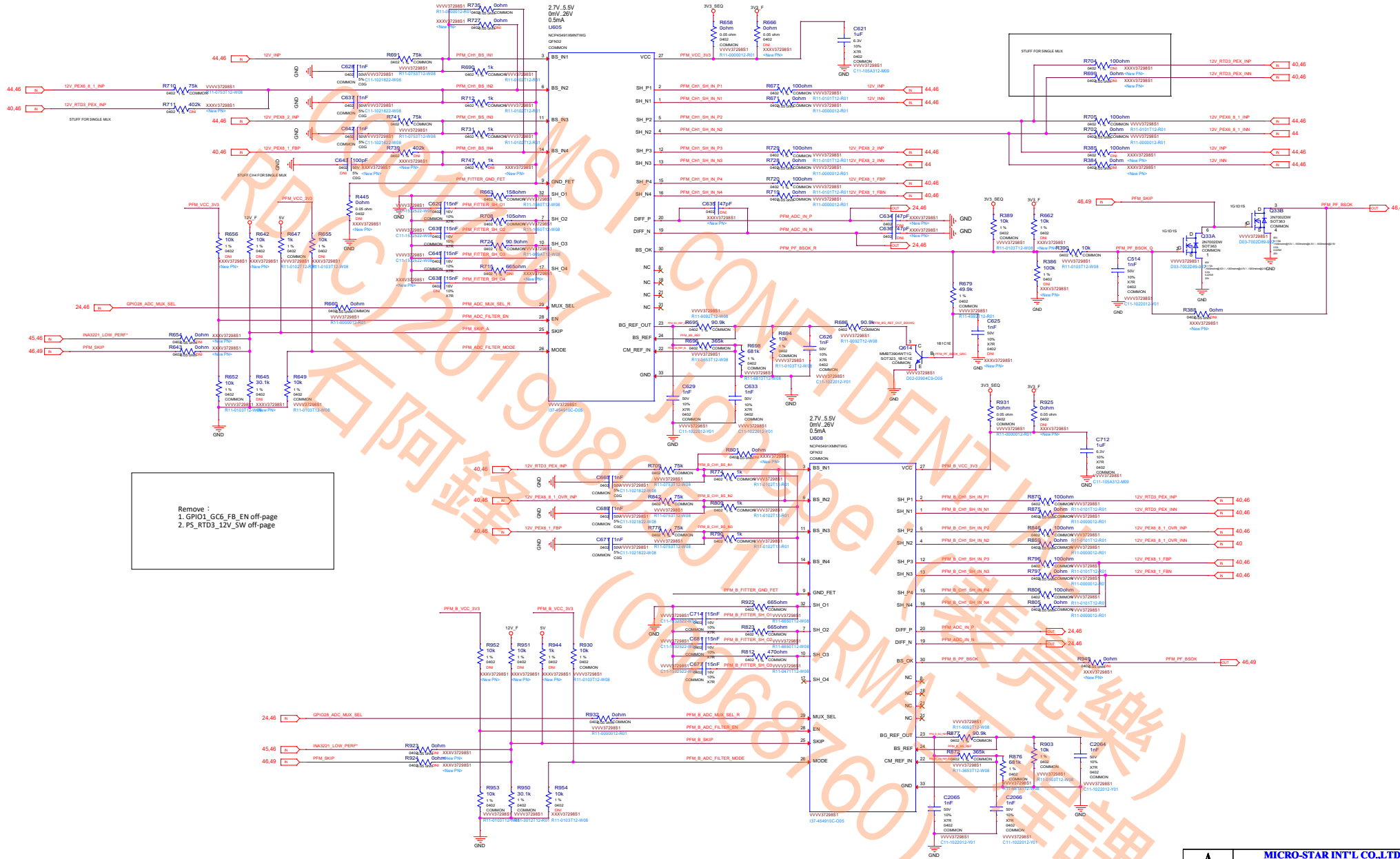


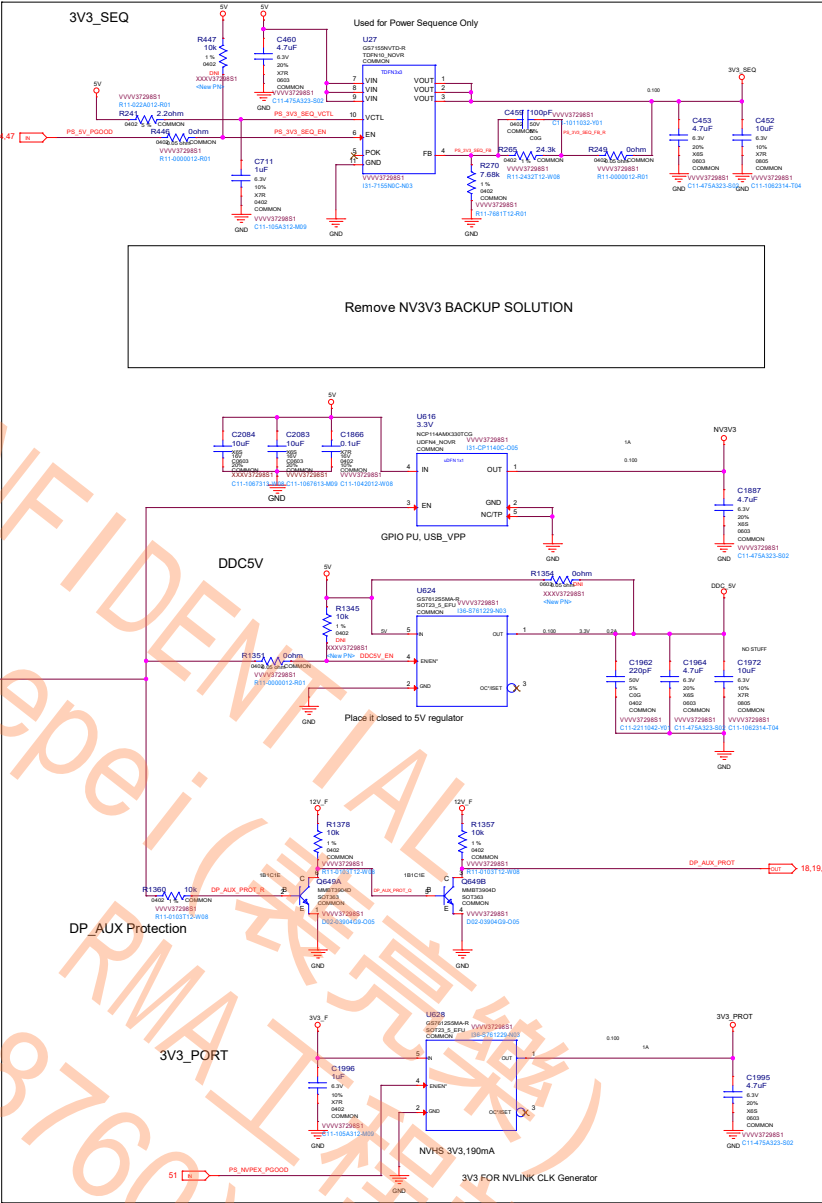
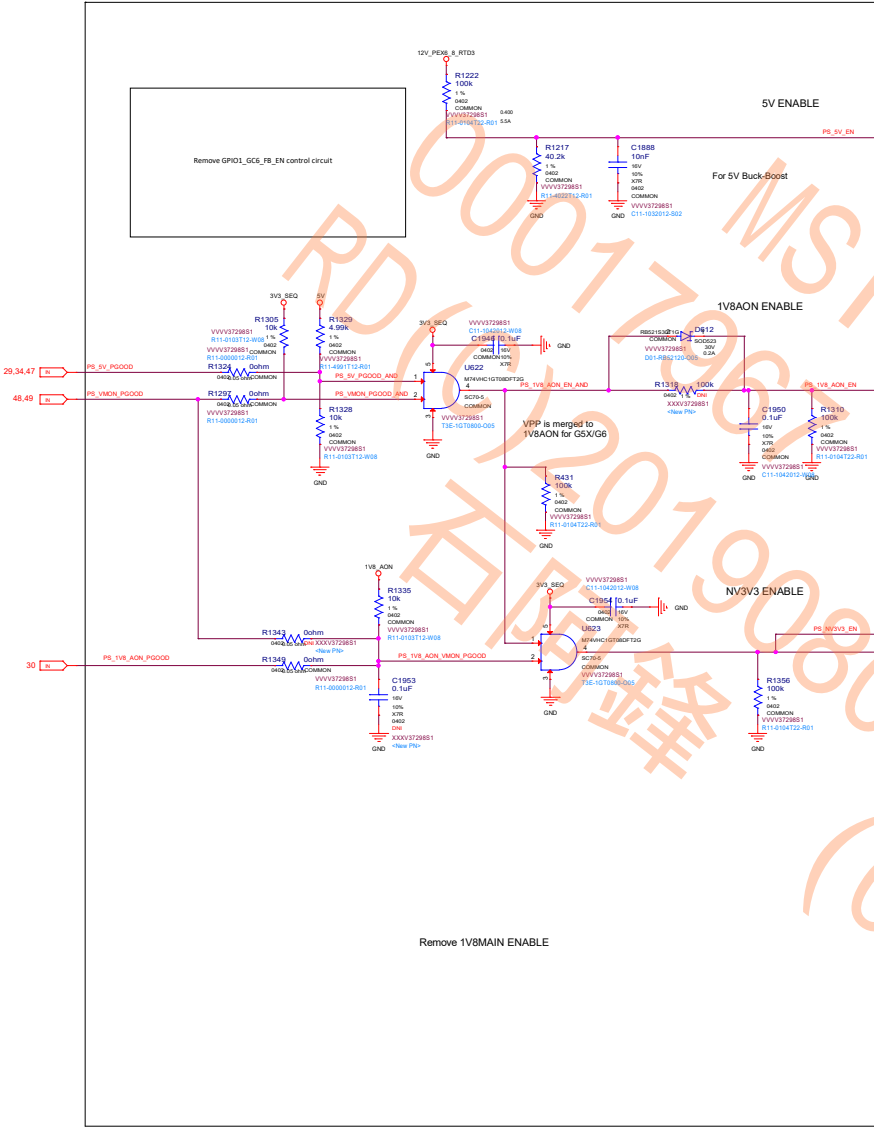


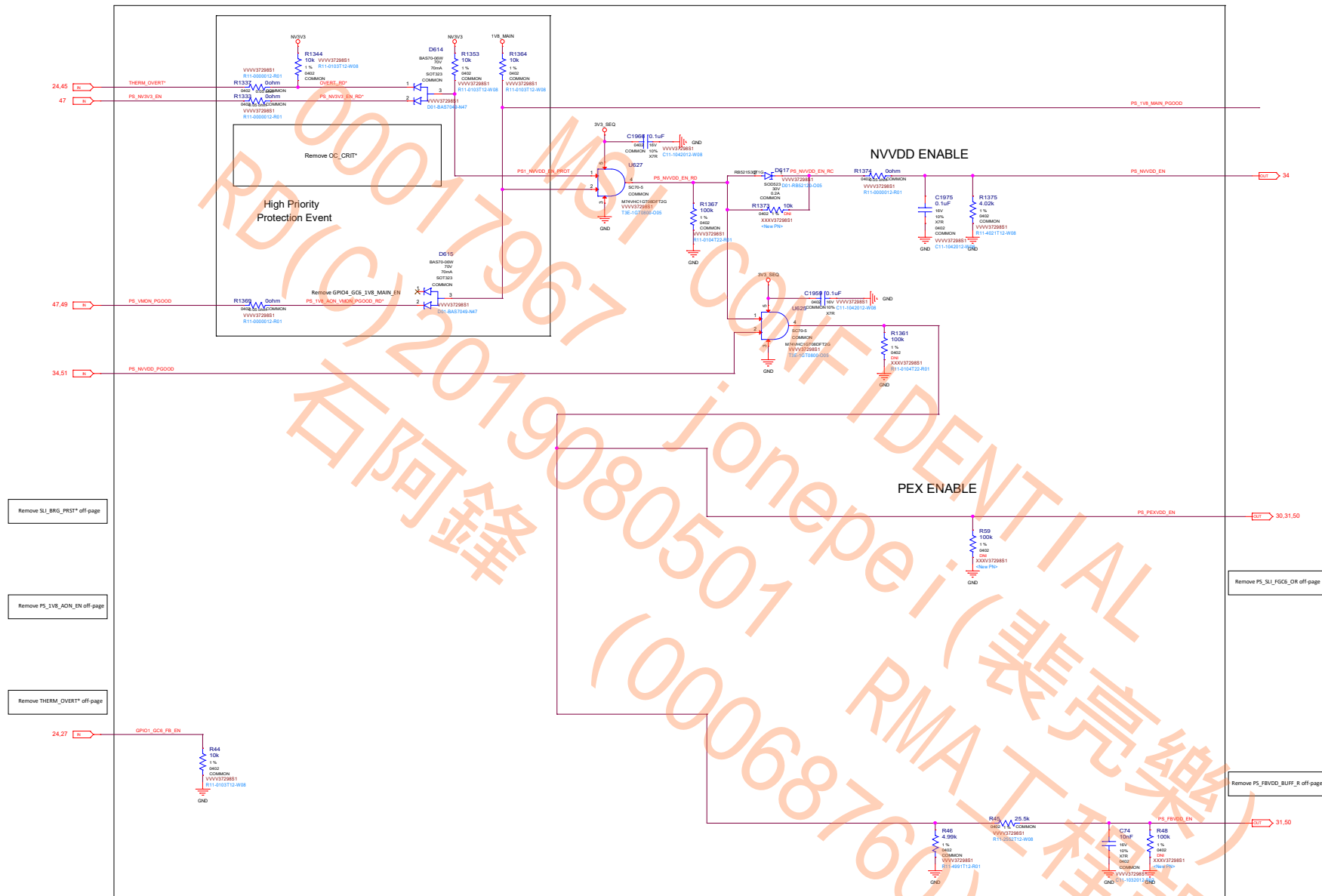
A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

GPIO12_LOW_PERP*	GPIO12_LOW_PERP*
0	Slow
1	Normal

STUFF IF USING 2KMUX

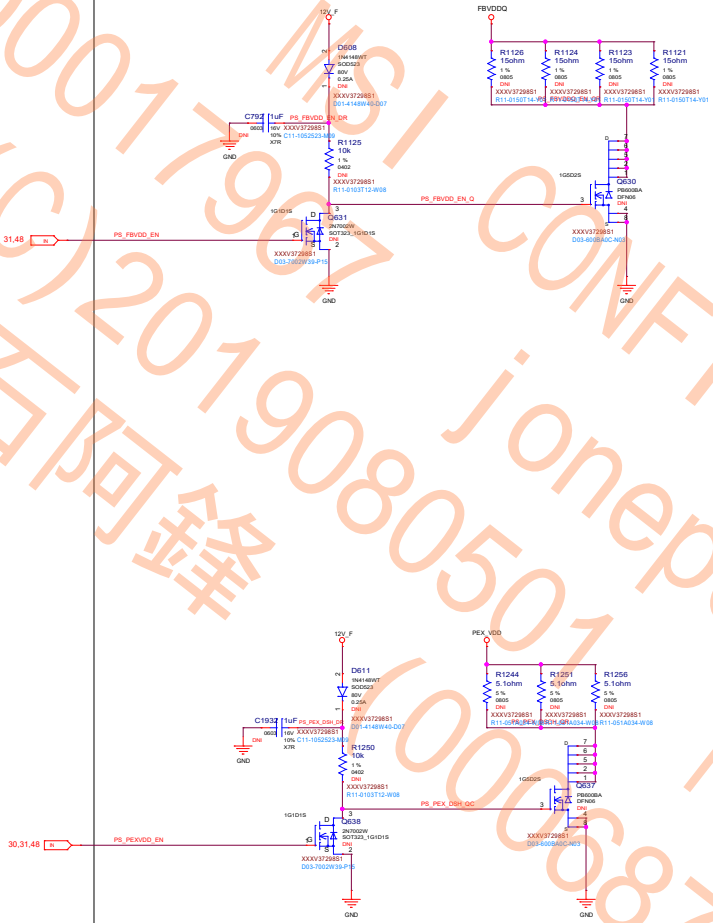


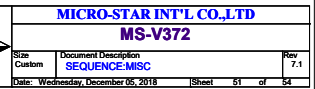
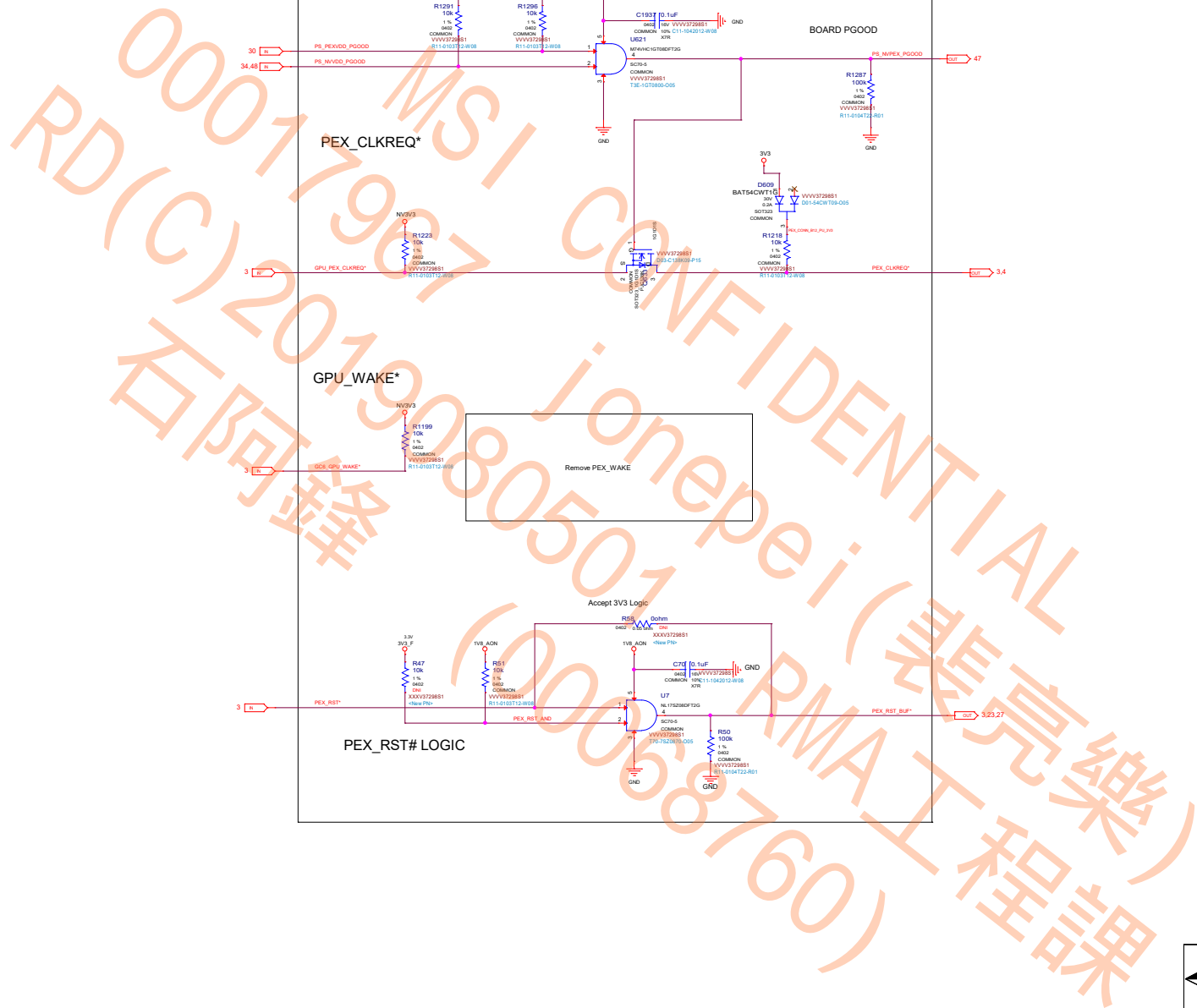


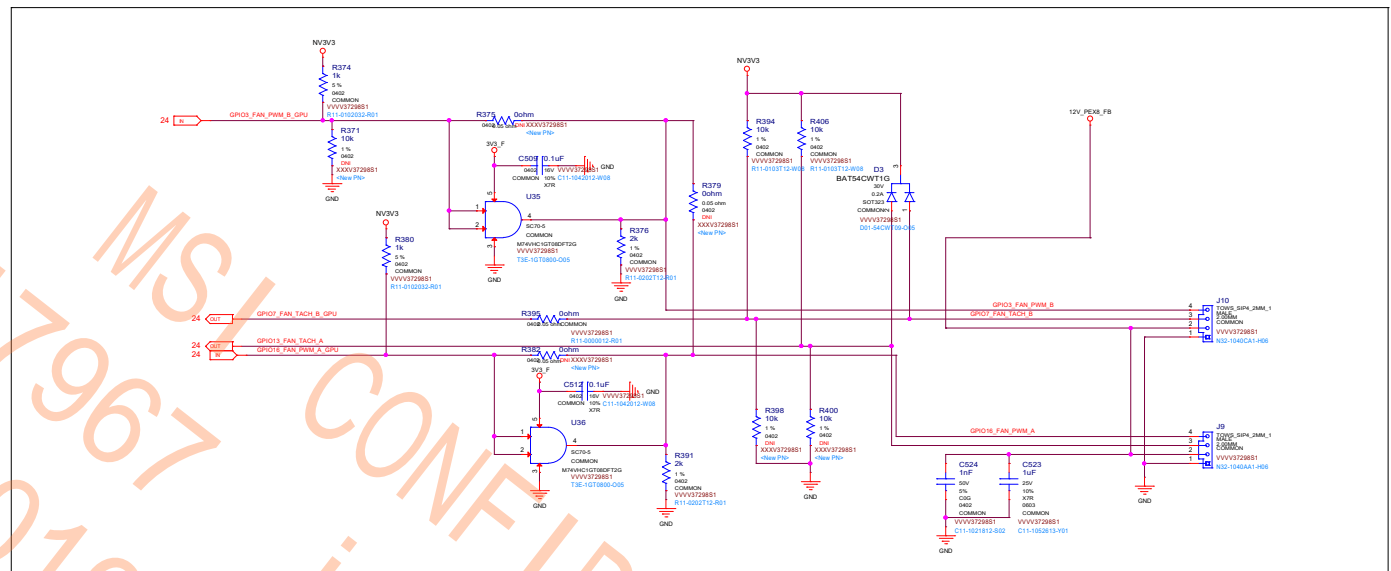


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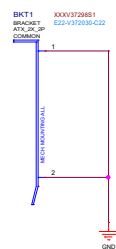
Remove LED BOOST



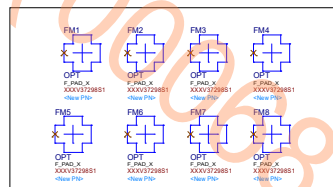
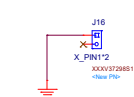
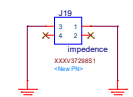
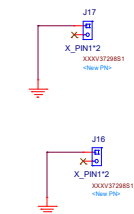
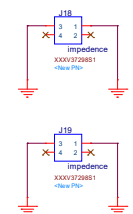
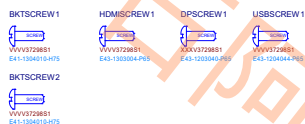
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Brackets:



Screw



Mechanical Holes Symbol

